

PCB Number:14130-1
ECO# number : 823507

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[illegible]

```
BOM Configuration
(R):Unmount
(C):Carrizo
(L):Carrizo-L
(D):Debug used
(I):Internal PSU(12V)
(E):External Adapter(19V)
(P):PCIex16
```

PCB BOARD SIZE

200mm X 267mm

-1 BUILD

AMD Carrizo/-L Platform

LAN : Gb LAN RTL811H

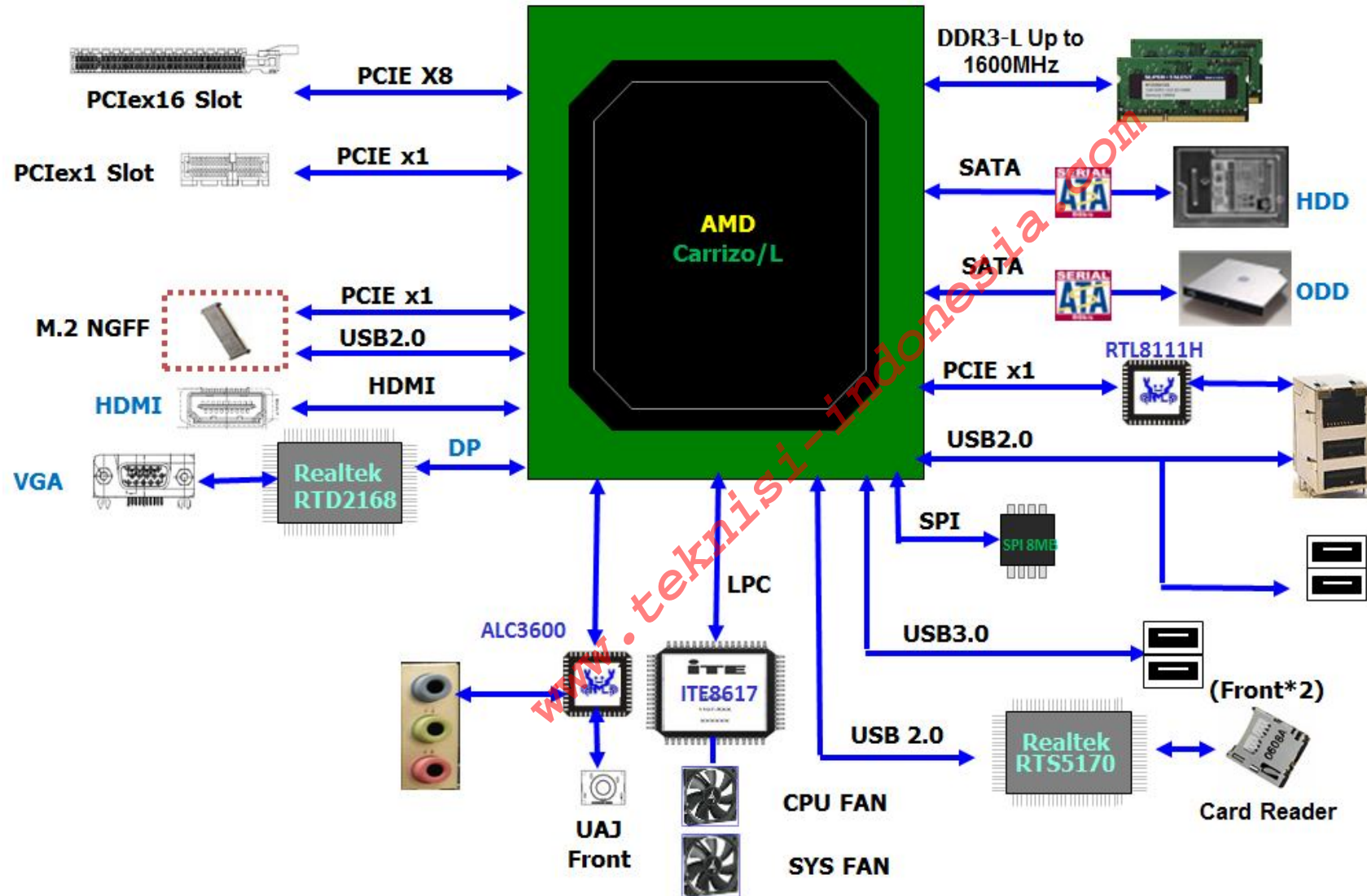
AUDIO: ALC3600

SIO:ITE8617

Project Name: Lily-MT
 Project Code: 3PD03B010001
 PCB Version: -1
 PCB Number :14130

PCB BOARD SIZE
 200mm X 267mm
 6 Layer

Internal Slot/Header
 Front/Rear IO
 Chipset



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Title

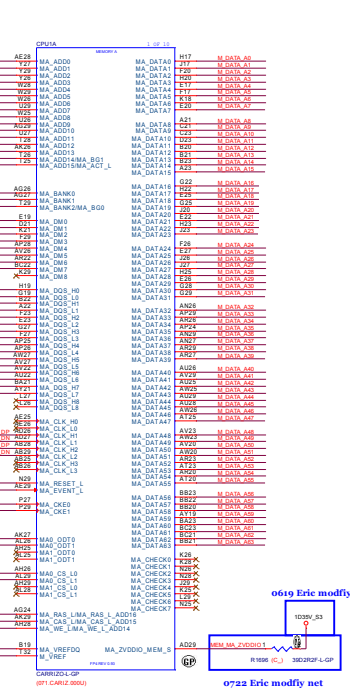
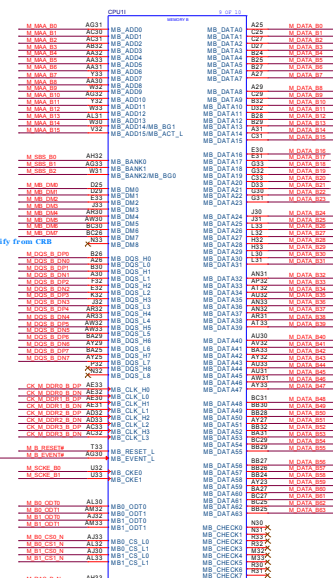
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Table 3. Valid Socketed-Memory ConfigurationsTable 13. Memory Feature Compatibility


5.1 Memory Interface

There are four signal groups for the memory bus interface—a Data group, a Control group, an Address/Command group, and a Clock group. The two types of FP4 processors support different memory configurations. See [Table 1](#) for a list of FP4 processor type feature sets.

- Type 1 processors have two DDR3 channels, labeled A and B.
- Type 2 processors have one DDR3 channel, labeled B.

See the sections that follow for memory package-specific and implementation-specific information and design considerations.

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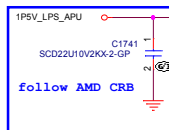
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Title Reserved		
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0618 Eric add
Type 2 (Carrizo-L) have no VDDCR_FCH power

CRB CAP: VDDBT_RTC G
1* 0.22uF 0402 X5R

AR17

power rail 1.5V



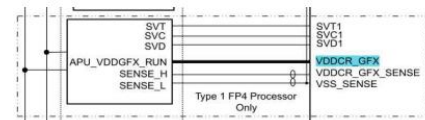
CARRIZO-L AP
(071.CARL.DWG)

FP4 REV 0.00

Type 2 (Carrizo-L) have no VDDCR_GFX power

12.3.1 CPU, Northbridge, and GPU Voltages

VDDCR_CPU is the voltage rail for the CPU core. VDDCR_NB powers the Northbridge and for FP4 Type 2 processors the integrated GPU circuitry. FP4 Type 1 processors have a separate VDDCR_GFX GPU power plane. The number of capacitors that can be placed on the layout is different depending on the via placement and power-plane cut. Vias connecting to capacitors should have masks up to the via hole. See Table 107 for a detailed list of required capacitors for VDDCR_CPU, VDDCR_NB, and VDDCR_GFX.



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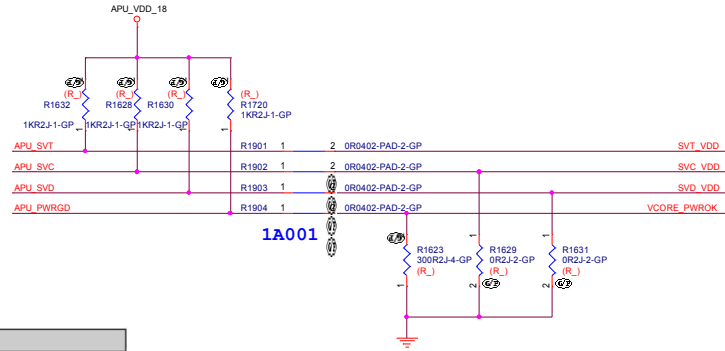
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Hsinchu, Taipei

007_APU_FP4 (POWER)

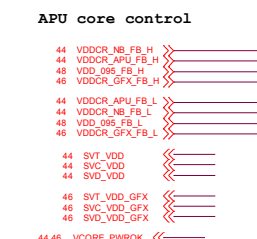
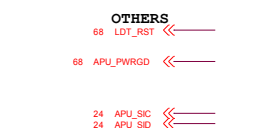
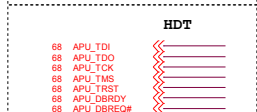
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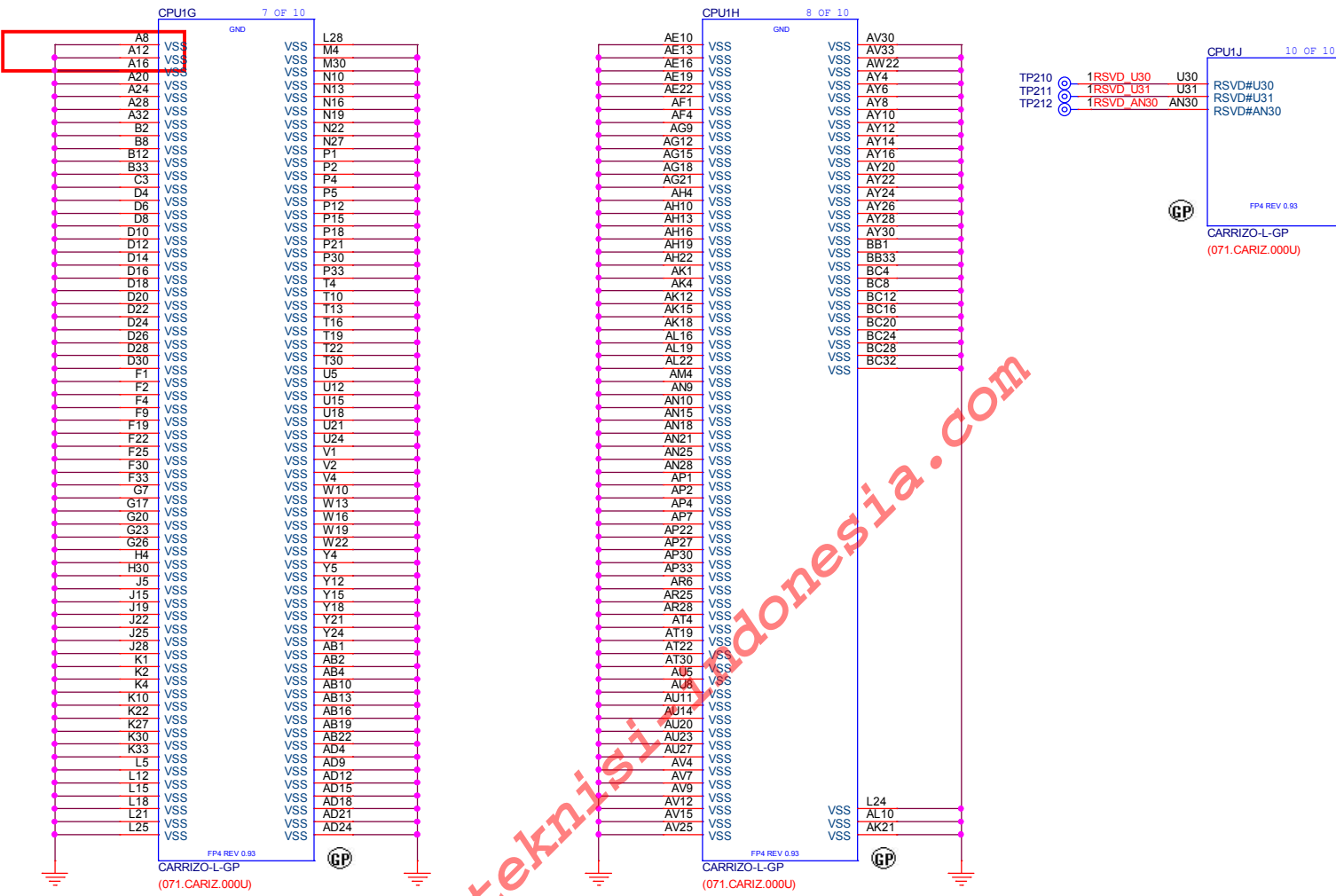
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no support for
type 2 processor (Carrizo-L)

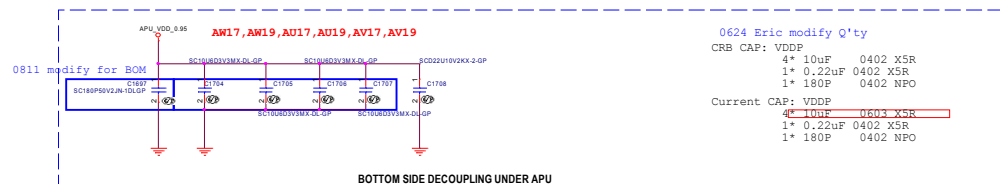
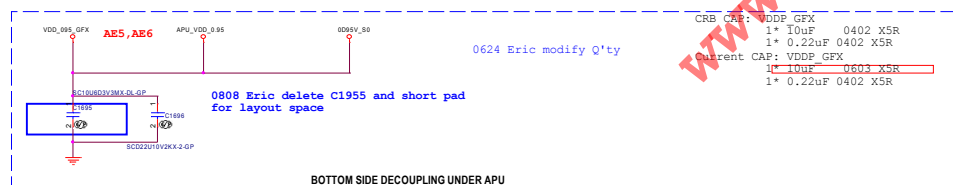
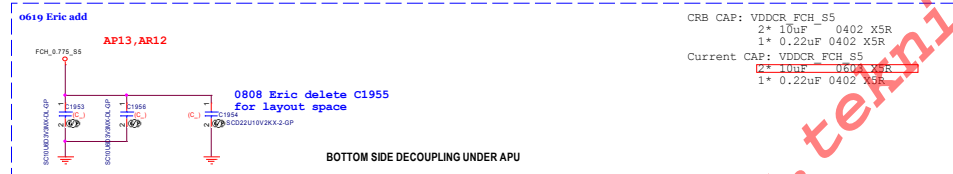
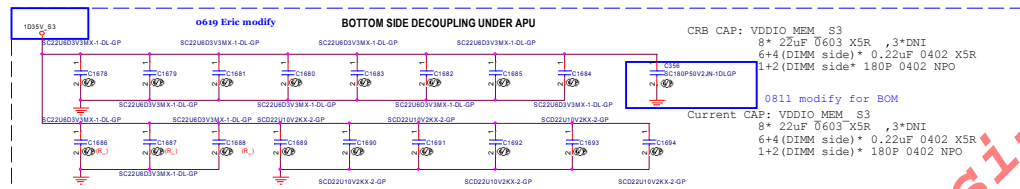
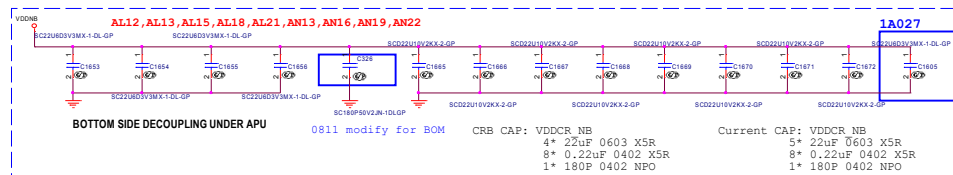
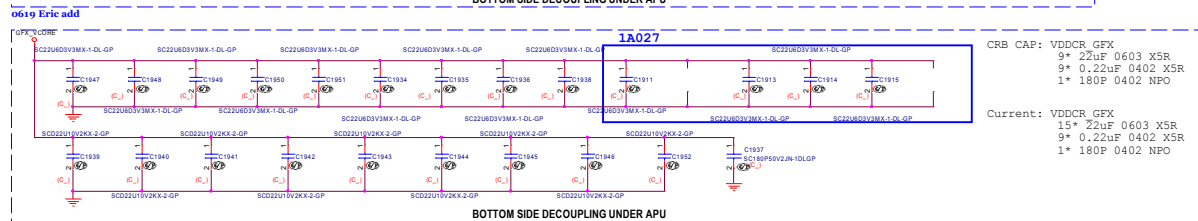
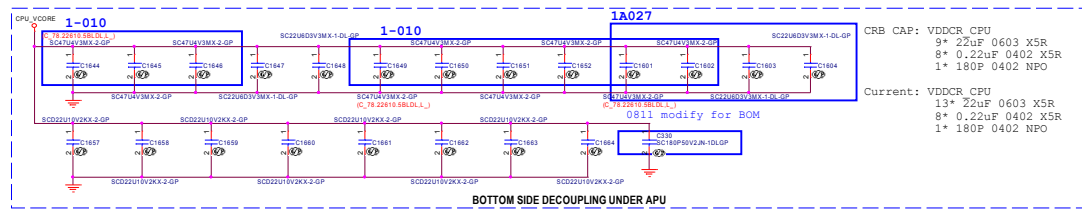


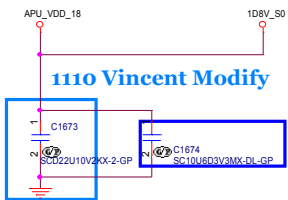
AMD CRB for socket



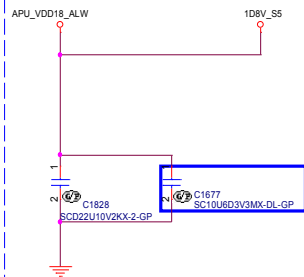
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Title		
009_APU_FP4 (VSS)		
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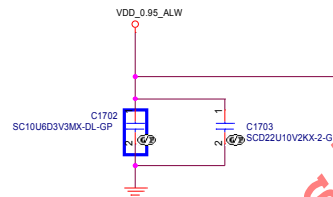


CRB CAP: VDDP_18
 1* 10uF 0402 X5R
 1* 22uF 0603 X5R
 Current CAP: VDDP_18
 1* 10uF 0603 X5R
 1* 22uF 0603 X5R



CRB CAP: VDDP_18_S5
 1* 10uF 0402 X5R
 1* 0.22uF 0402 X5R
 Current CAP: VDDP_18_S5
 1* 10uF 0603 X5R
 1* 0.22uF 0402 X5R

AN12, AP12



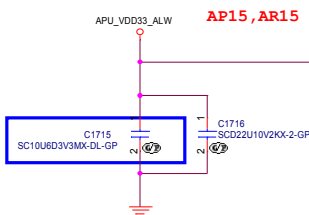
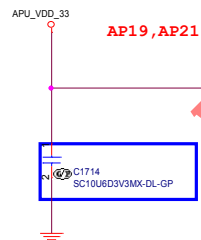
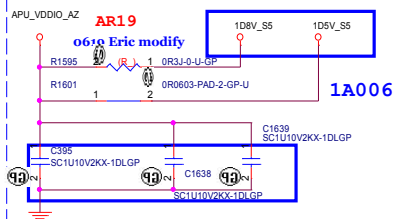
CRB CAP: VDDP_S5
 1* 10uF 0402 X5R
 1* 0.22uF 0402 X5R
 Current CAP: VDDP_S5
 1* 10uF 0603 X5R
 1* 0.22uF 0402 X5R

delete for 0.95V_DUAL power rail, no use 0.95V_DUAL from CRB

CRB CAP: VDDIO_AUDIO
 3* 1uF 0402 X5R
 Current CAP: VDDIO_AUDIO
 3* 1uF 0402 X5R

CRB CAP: VDD_33
 1* 10uF 0402 X5R
 Current CAP: VDD_33
 1* 10uF 0603 X5R

CRB CAP: VDD_33_S5
 1* 10uF 0402 X5R
 1* 0.22uF 0402 X5R
 Current CAP: VDD_33_S5
 1* 10uF 0603 X5R
 1* 0.22uF 0402 X5R



0624 Eric delete

0624 Eric delete

DDR DATA

5.12 M_DATA_B0_63
5.12 M_DQS_B_DP0_7
5.12 M_DQS_B_DM0_7
5.12 M_MB_DM7_0

DDR CMD/ADD

5.12 M_MAA_B0_15
5.12 M_WE_B_N
5.12 M_CAS_B_N
5.12 M_RAS_B_N
5.12 M_SBS_B0
5.12 M_SBS_B1
5.12 M_SBS_B2

DDR CTRL

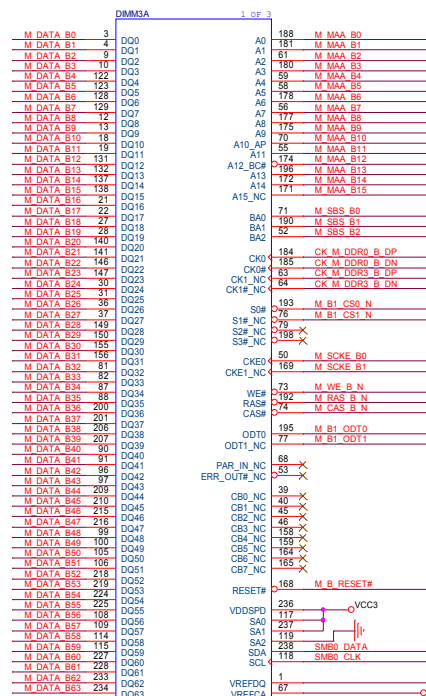
5 M_B1_CS0_N
5 M_B1_CS1_N
5 M_SCKE_B0
5 M_SCKE_B1
5 M_B1_ODT0
5 M_B1_ODT1

DDR CLOCK

5 CK_M_DDR0_B_DP
5 CK_M_DDR0_B_DN
5 CK_M_DDR3_B_DP
5 CK_M_DDR3_B_DN

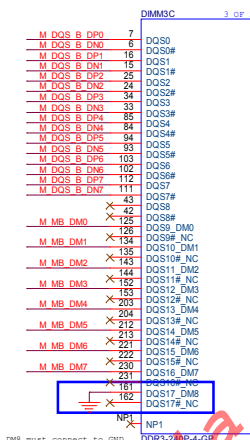
DDR OTHERS

5.12 M_B_RESET#
12.14.18 SMB0_CLK
12.14.18 SMB0_DATA
5.12 M_B_EVENT#

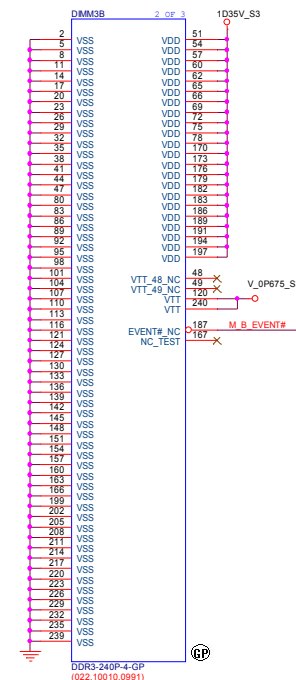


DDR3-240P-4-GP
(022.10010.0991)
Black color
Pin height is 2.7mm

Trace: 12/12 mils
C1727(R_)
SC1U10V2KX-1DLGP
C1750
SC1U10V2KX-1DLGP
C16
SC1U10V2KX-1DLGP



SMBUS Address: 011



1A025

DDR DATA

5 M_DATA_A0_631 <<<
5 M_DQS_A_DP0_7 <<<
5 M_DQS_A_DP0_7 <<<
5 M_MAA_DM7_0 <<<

DDR CMD/ADD

5 M_MAA_A0_15 <<<

5 M_WE_A_N <<<
5 M_CAS_A_N <<<
5 M_RAS_A_N <<<

DDR CTRL

5 M_A0_CS0_N <<<
5 M_A0_CS1_N <<<
5 M_SCKE_A0 <<<
5 M_SCKE_A1 <<<
5 M_A0_ODT0 <<<
5 M_A0_ODT1 <<<

DDR CLOCK

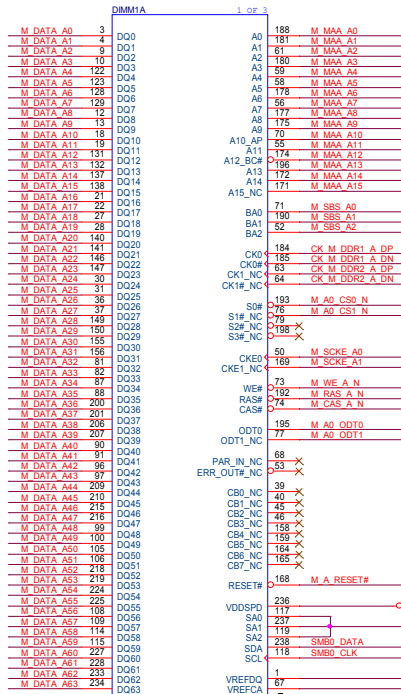
5 CK_M_DDR2_A_DP <<<
5 CK_M_DDR2_A_DP <<<
5 CK_M_DDR1_A_DP <<<
5 CK_M_DDR1_A_DP <<<

DDR OTHERS

5 M_A_RESET# <<<

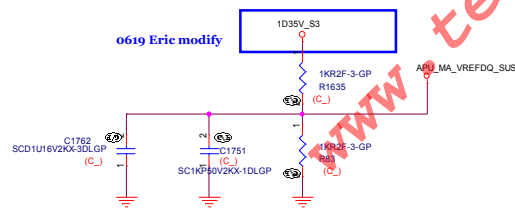
12,13,18 SMB0_CLK <<<
12,13,18 SMB0_DATA <<<

5 M_A_EVENT# <<<

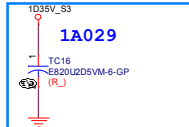
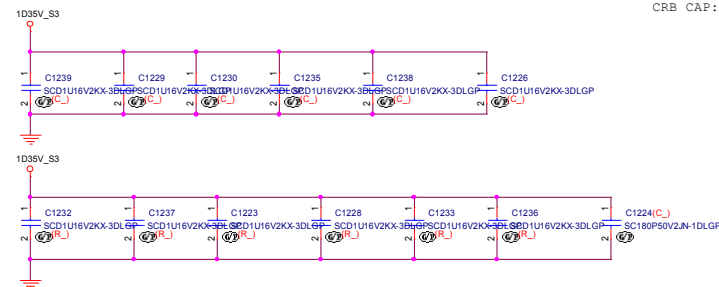


OTES Part number: 22.10220.801

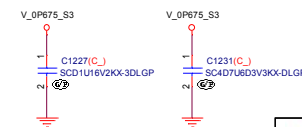
DE-COUPLING FOR CHANNEL A DIMM



1A026



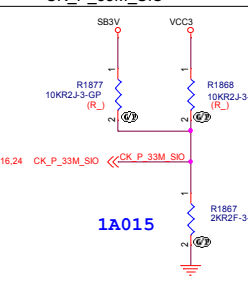
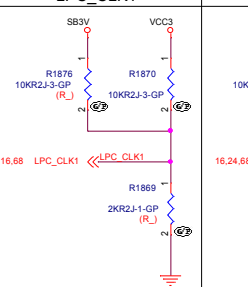
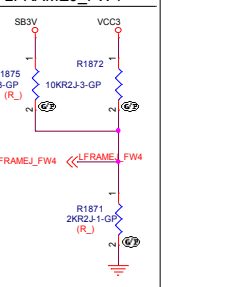
1016 Vincent modify
Change 100uF*2 to 820uF*1



CRB CAP: VDDIO MEM_S3
12* 0.1uF ,6*DNI
2* 100uF 0402 X5R
1* 180P 0402 NPO

+MEM_VTT
1* 0.1uF
1* 4.7uF

Strap Pin For TYPE 2 (Carrizo-L)

Description	LPC_CLK0	LPC_CLK1	LFRAME_L
GPIO	CK_P_33M_SIO	LPC_CLK1	LFRAMEJ_FW4
Schematic			
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 48Mhz crystal clock and generate both internal and external clocks (DEFAULT)	SPI ROM (DEFAULT)
PULL LOW	BOOT FAIL TIMER DISABLED (DEFAULT)	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	LPC ROM

Strap Pin For TYPE 1 (Carrizo)

0623 Eric modfiy

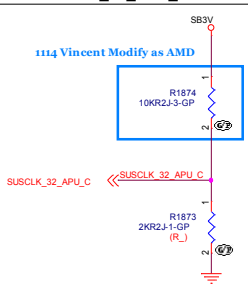
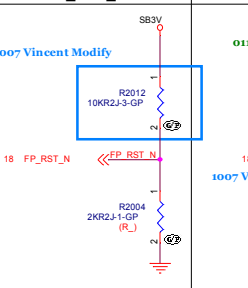
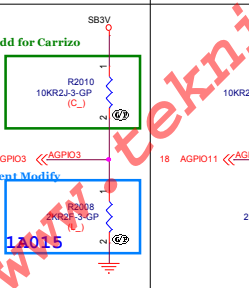
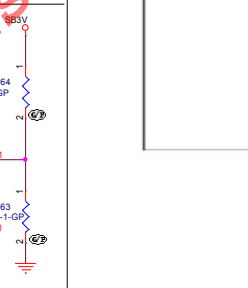
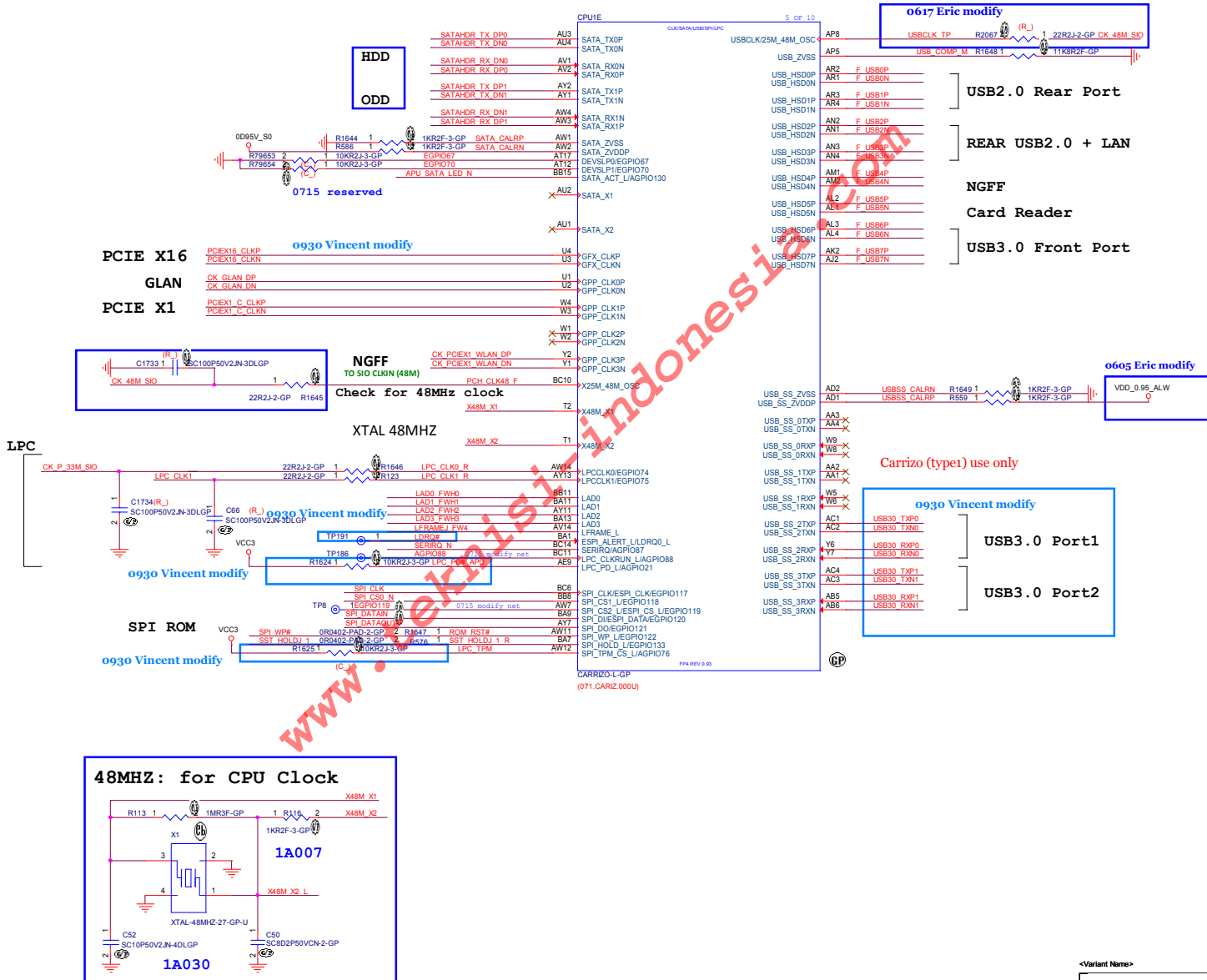
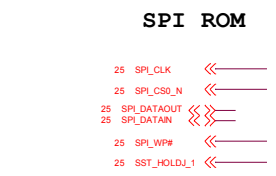
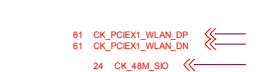
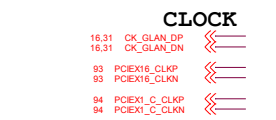
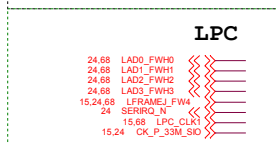
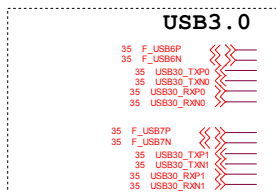
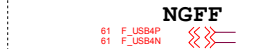
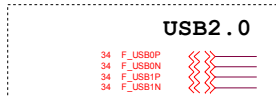
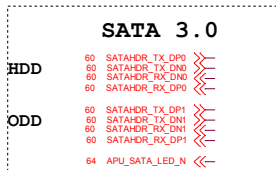
Description	RTC_CLK Int pull-up	SYS_RSET_L	AGPIO3	BLINK
GPIO	SUSCLK_32_APU_C	FP_RST_N	AGPIO3	AGPIO11
Schematic				
PULL HIGH	RTC coin Battery is implemented (DEFAULT)	normal reset mode (DEFAULT)	Enhanced Reset logic (Default) for faster resume from S5	LDT_RST#/LDT_PWRGD output to APU (DEFAULT)
PULL LOW	RTC coin Battery is not implemented	short reset mode	Traditional Reset logic (DEFAULT)	LDT_RST#/LDT_PWRGD output to Pads

Table 90. Strapping Options

SIGNAL Name	Strap Name	Type	Default Value	Bit Value	Description
LFRAME_L	ROMTYPE	II	1	0	LPC ROM
				1	SPI ROM (Default)
LPCLK1	CLKGEN	II	1	0	Reserved
				1	Configured for internal clock-generator (Default)
LPCLK0	BOOTFAILTIMER	II	0	0	Boot Fail Timer Disabled (Default)


Table 90. Strapping Options (continued)

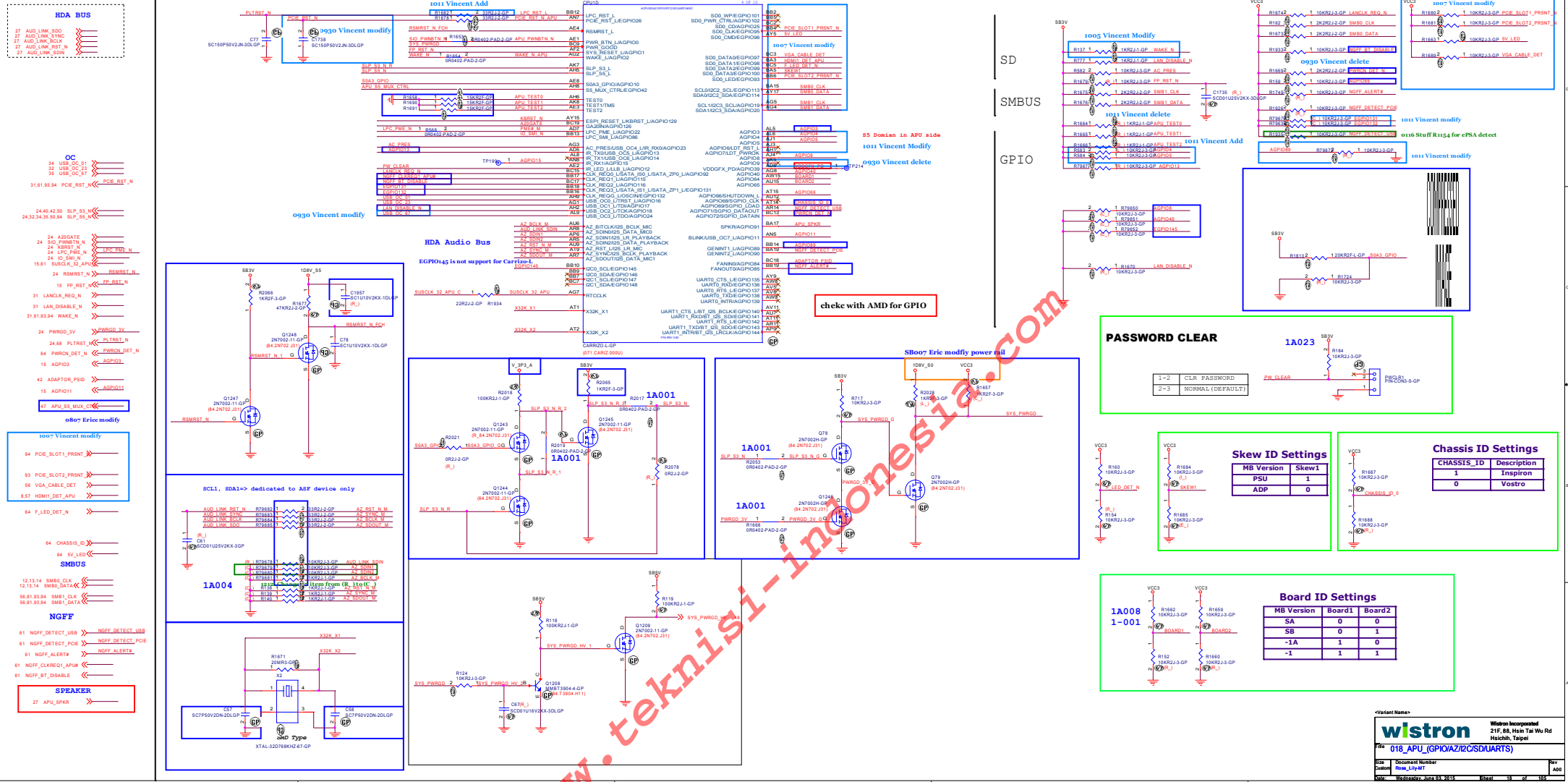
SIGNAL Name	Strap Name	Type	Default Value	Bit Value	Description
LPCLK0	BOOTFAILTIMER	II	0	1	Boot Fail Timer Enabled
RTCCLK	RTC Coin Battery	I	1	0	RTC Coin Battery is not implemented
				1	RTC Coin Battery is implemented (Default)
SYS_RESET_L	ShortReset	I	1	0	Reserved
				1	Normal powerup/reset timing (Default)
AGPIO3	Alternate Reset	I	1	0	Traditional Reset logic (Type 1 FP4 Processor Only) 2 kΩ (± 5%) pull-down resistor to VSS
				1	Enhanced Reset logic (Default) for faster resume from S5 10 kΩ (± 5%) pull-up resistor to VDD_33_S5
<p>Note:</p> <ul style="list-style-type: none"> Platforms that are designed for AOAC complaint are recommended to use Alternate Reset To ensure the strap can capture correct information, platform has to make sure AGPIO3 has valid voltage config value until 20 ms after RsmRstB has risen to at least 3.0 v. 					



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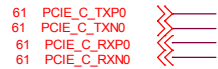
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PCIE X16



NGFF



PCIE X1

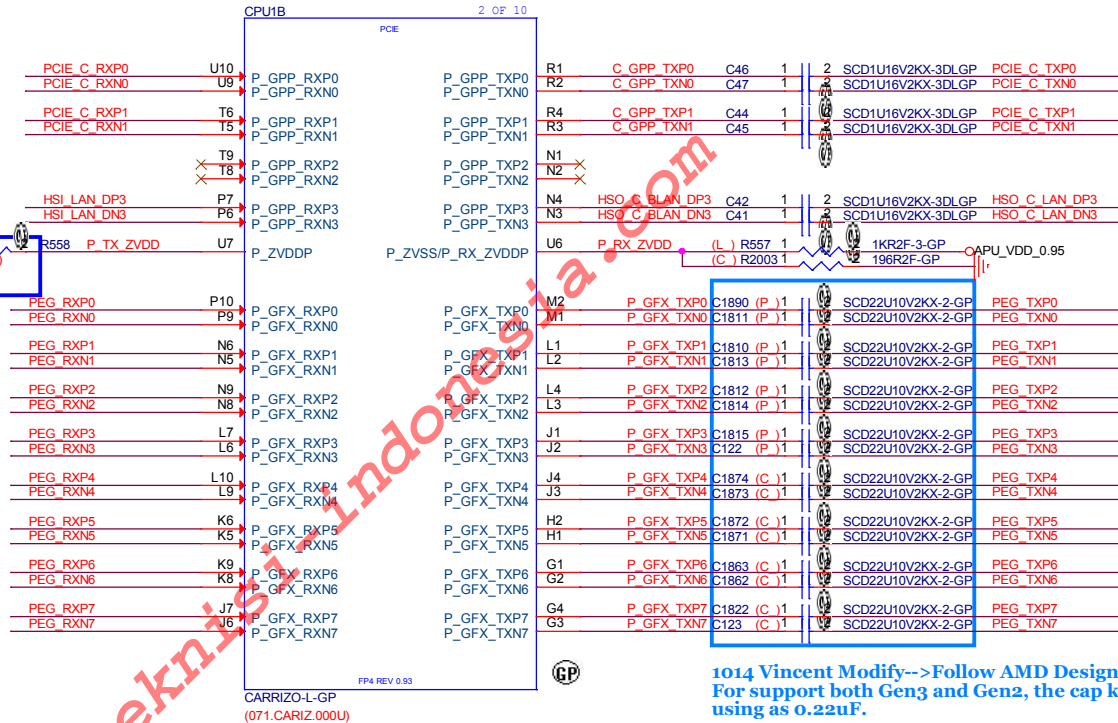


Giga LAN



0625 Eric modify

APU_VDD_0.95 1K69R2F-2-GP1 (C_64.19605.6DL.L)
Type1 Carrizo use 196 ohms
Type2 Carrizo-L use 1.69k ohms



NGFF

PCIE X1

Giga LAN

0619 Eric modify

PCIE X16

	Type1	Type2	Type1	Type2		
P_ZVDDP	A	Pull-up resistor	196Ω (± 1%)	1.69 kΩ (± 1%)	-	VDDP
P_ZVSS/ P_RX_ZVDD P	A	Pull-down resistor	Pull-up resistor	196Ω (± 1%)	1 kΩ (± 1%)	VSS VDDP

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Title 019_APU_FP4(PCIE I/F)

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Title	Description	Status	Priority	Due Date	Assignee	Owner	Created	Updated	Comments
1	Project A	In Progress	High	2023-12-31	John Doe	John Doe	2023-10-01	2023-10-26	Initial setup
2	Project B	On Hold	Medium	2024-01-15	Jane Smith	Jane Smith	2023-09-15	2023-10-26	Waiting for funding
3	Project C	Planned	Low	2024-03-01	Mike Johnson	Mike Johnson	2023-10-01	2023-10-26	Research phase
4	Project D	Completed	Low	2023-08-31	John Doe	John Doe	2023-07-01	2023-10-26	Final review
5	Project E	In Progress	High	2023-11-30	Jane Smith	Jane Smith	2023-10-01	2023-10-26	Development phase

Reserved


Size	Document Number
Custom	Rosa_Lily-MT

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SPI ROM

- 16 SPI_CLK >>>
- 16 SPL_CS0_N >>>
- 16 SPI_DATAOUT >>>
- 16 SPI_DATAIN >>>
- 16 SPI_WP# >>>
- 16 SST_HOLDJ_1 >>>

SPI .ROM

SPI ROM

1A001

0626 Eric modify 330ohms Res to 0 ohm

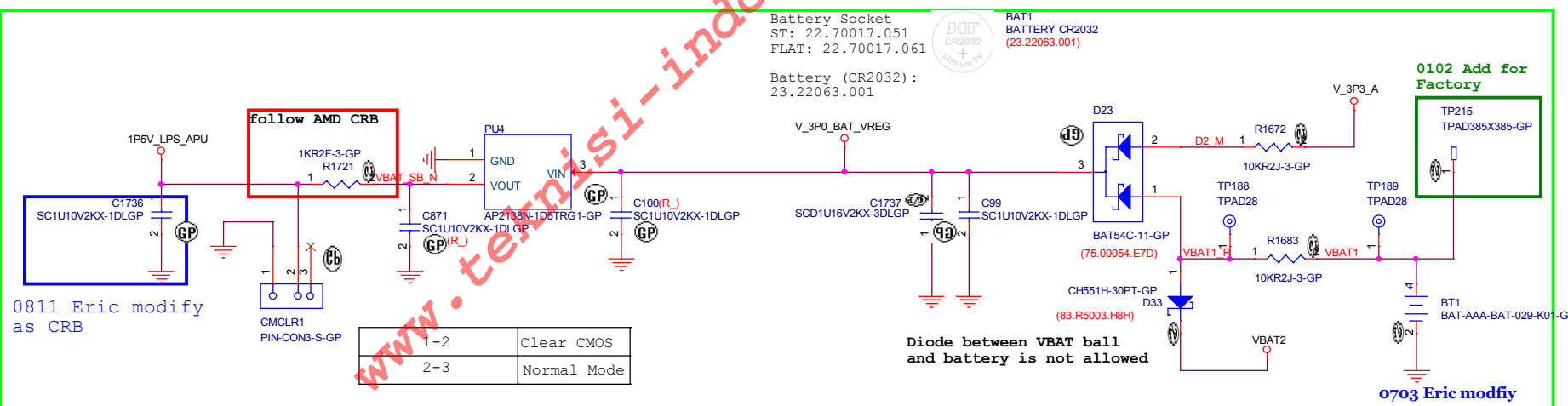
WP# function is not supported when SPI ROM is used on descriptor mode.

SOP8 for 8Mb

SA 0917 Eric modify BIOS P/N

SPI socket mount in SA stage

RTC



<Variant Name>

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Title 025_Flash ROM/RTC

Size B

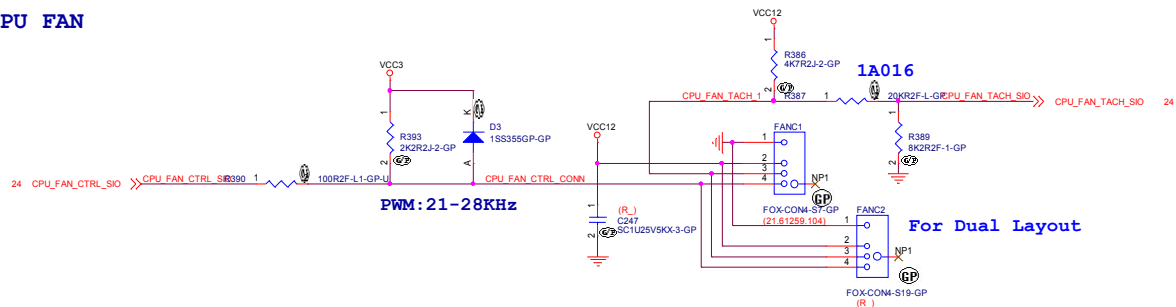
Document Number
Rosa_Lily-MT

Rev
A00

Date: Wednesday, June 03, 2015

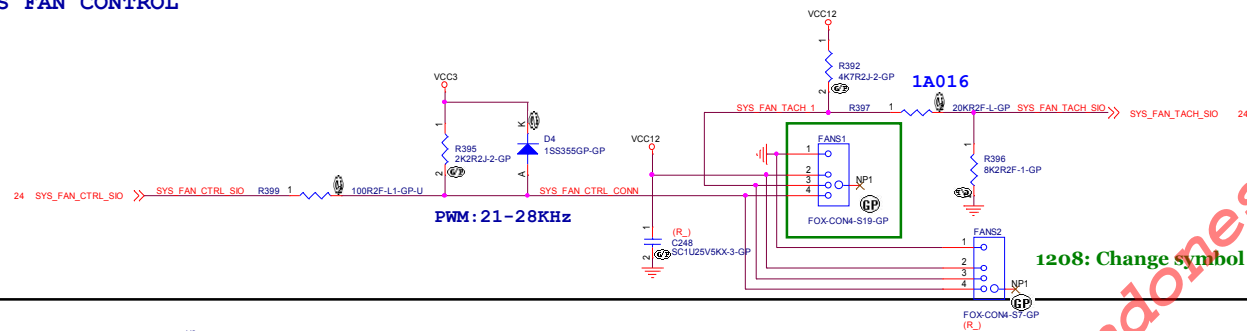
Sheet 25 of 105

CPU FAN



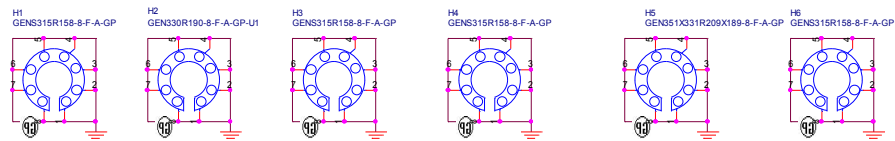
1014 Vincent Delete FAN control circuit

SYS FAN CONTROL

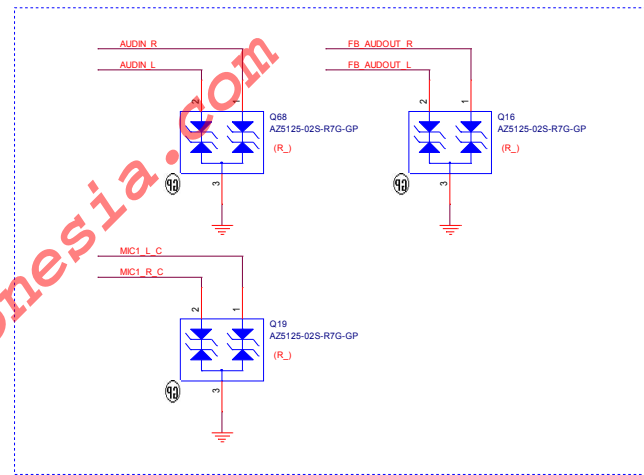
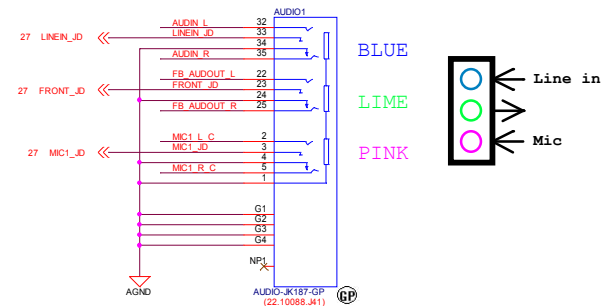
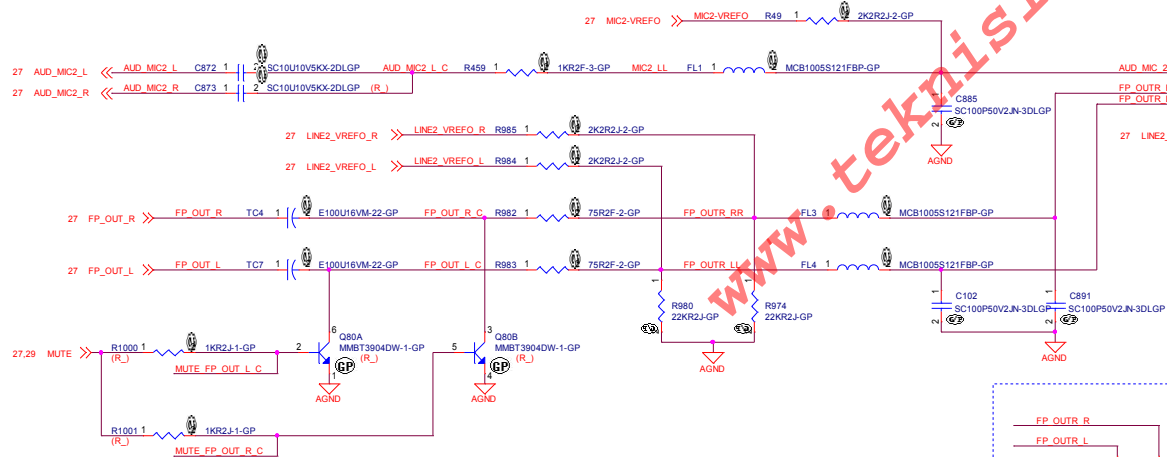
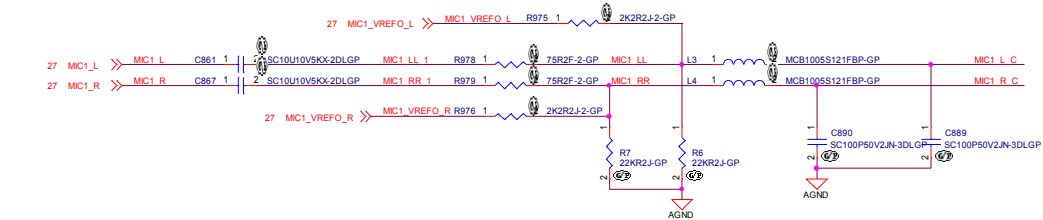
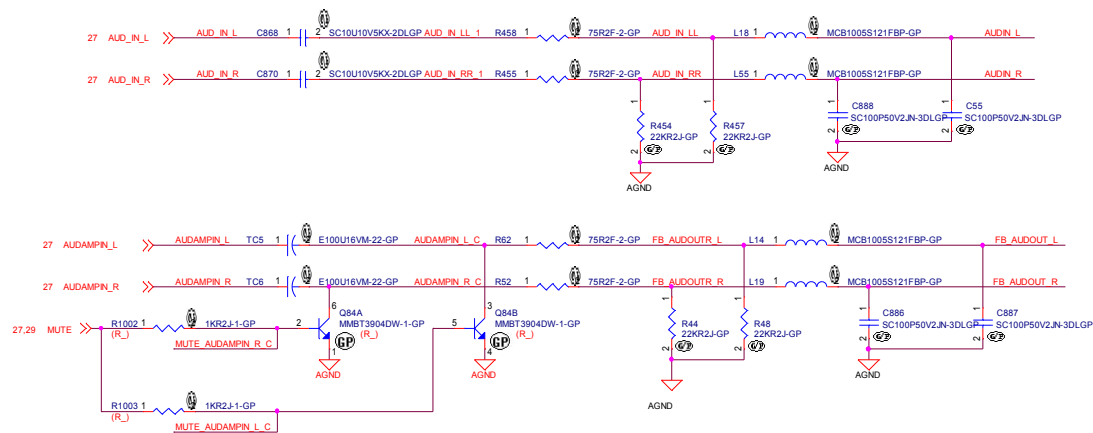


1014 Vincent Delete FAN control circuit

1208: Change symbol to 021.60234.0104 dark red part



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4-pin 3.5mm Headset Connector Pinout

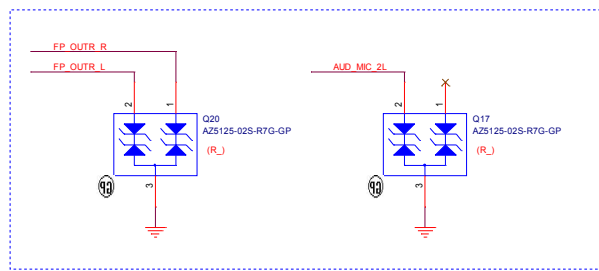


Nokia, Lenovo mobile		
Pin Number	Pin Name	Description
1	Tip	Left Audio Out
2	Ring-1	Right Audio Out
3	Ring-2	Microphone
4	Sleeve	Ground / Common


iPhone, Samsung, Blackberry, HTC		
Pin Number	Pin Name	Description
1	Tip	Left Audio Out
2	Ring-1	Right Audio Out
3	Ring-2	Ground / Common
4	Sleeve	Microphone

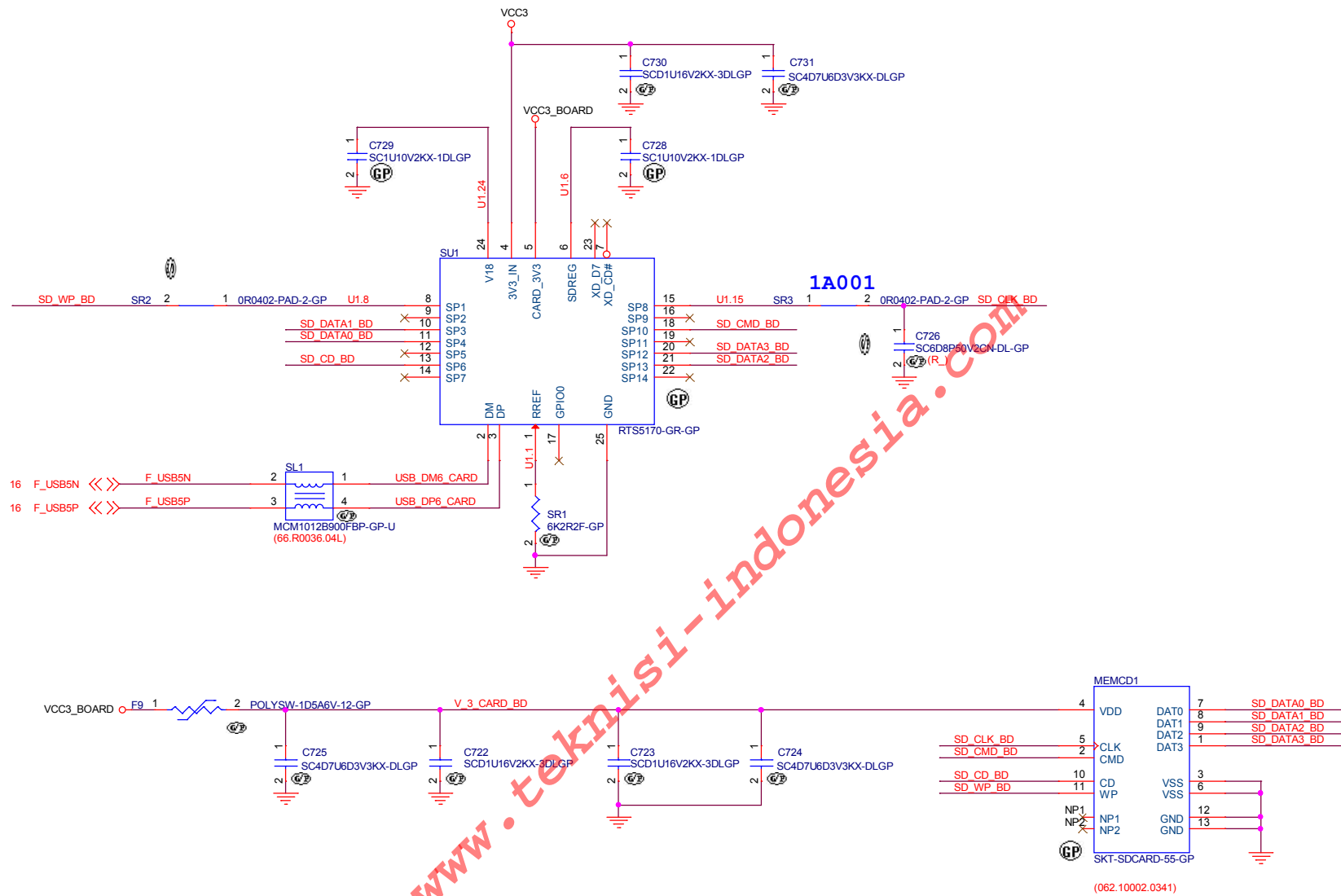
CTIA (Apple) Standard Headset

oTip: Left audio
oRing1: Right audio
oRing2: Ground
oSleeve: Microphone



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<Variant Name>

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Title **033_CardReader RTS5170**

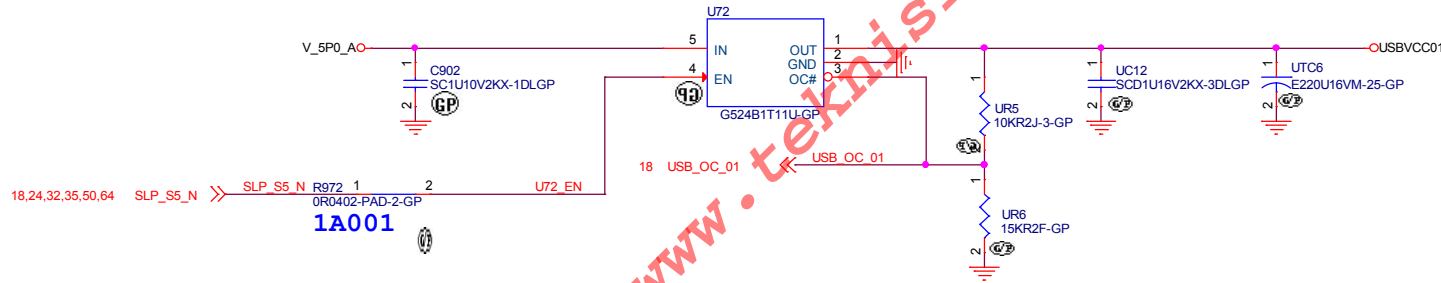
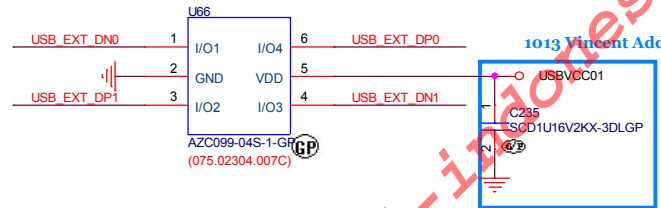
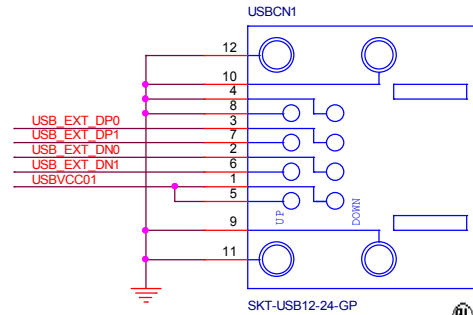
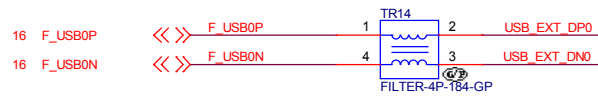
Size B Document Number
Rosa_Lily-MT

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A00

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Rear Port USB2.0



<Variant Name>

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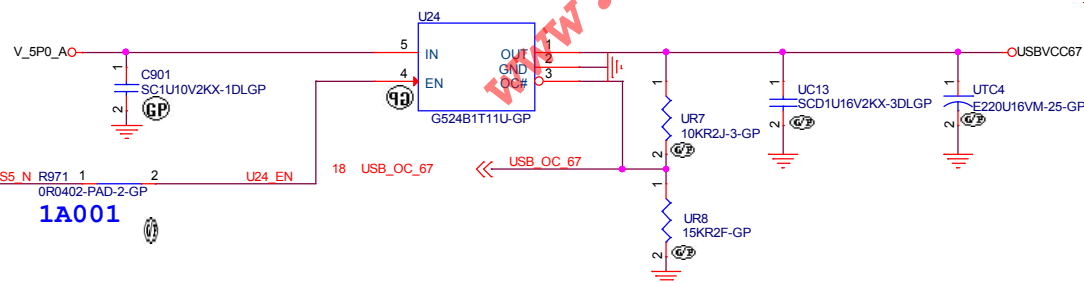
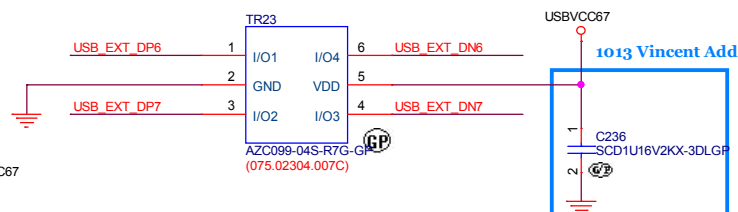
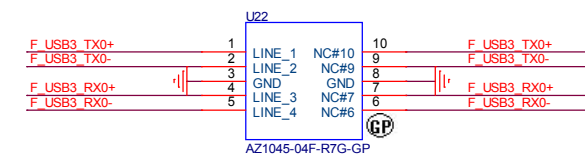
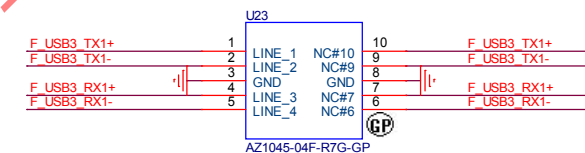
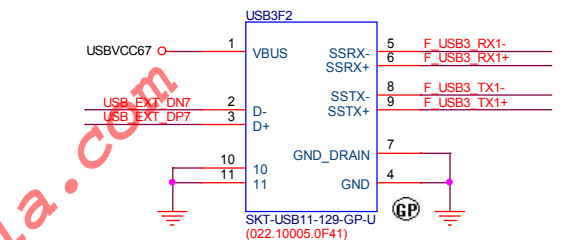
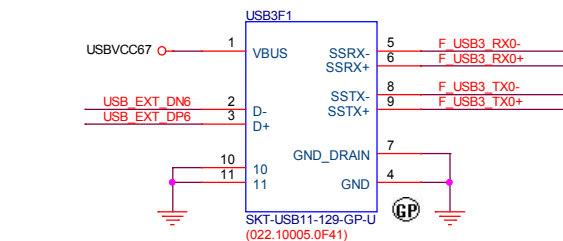
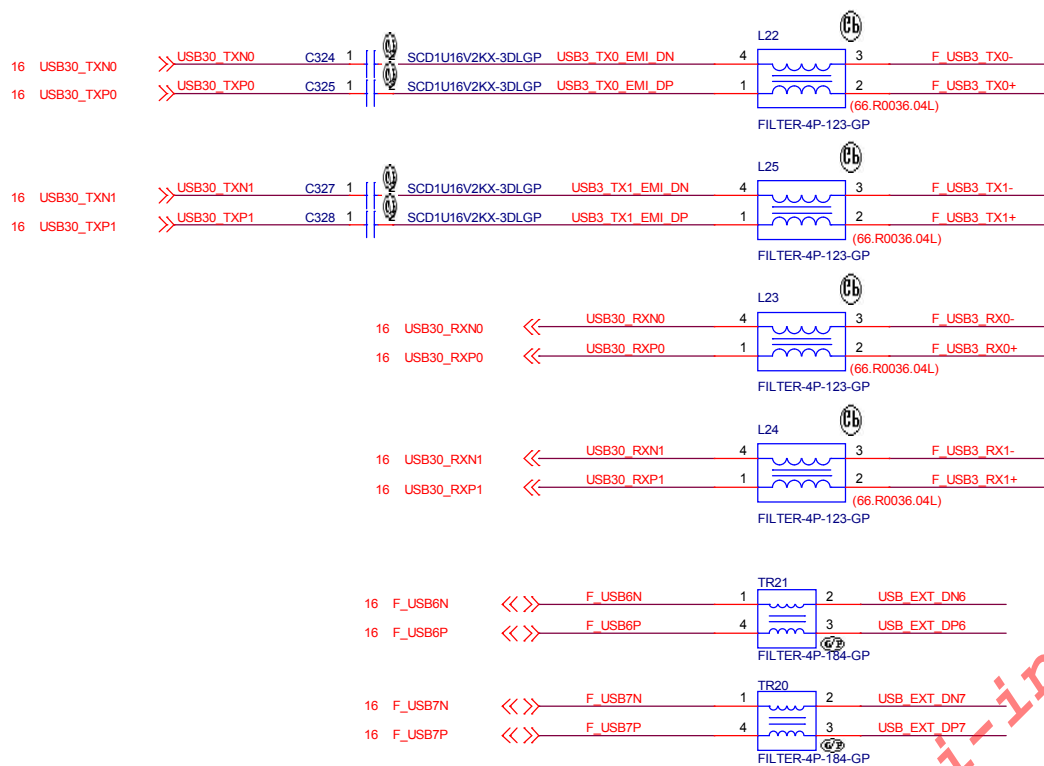
Title 034_Rear USB2.0

Size B Document Number
Rosa_Lily-MT

Rev
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<Variant Name>

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Title 035_Front USB3.0

Size B Document Number Rosa_Lly-MT

Rev A00


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<Variant Name>	
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File Reserved	
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<Variant Name>

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Title Reserved		
Size A	Document Number Rosa_Lily-MT	Rev A00
Date: Wednesday, June 03, 2015		
Sheet 39 of 105		

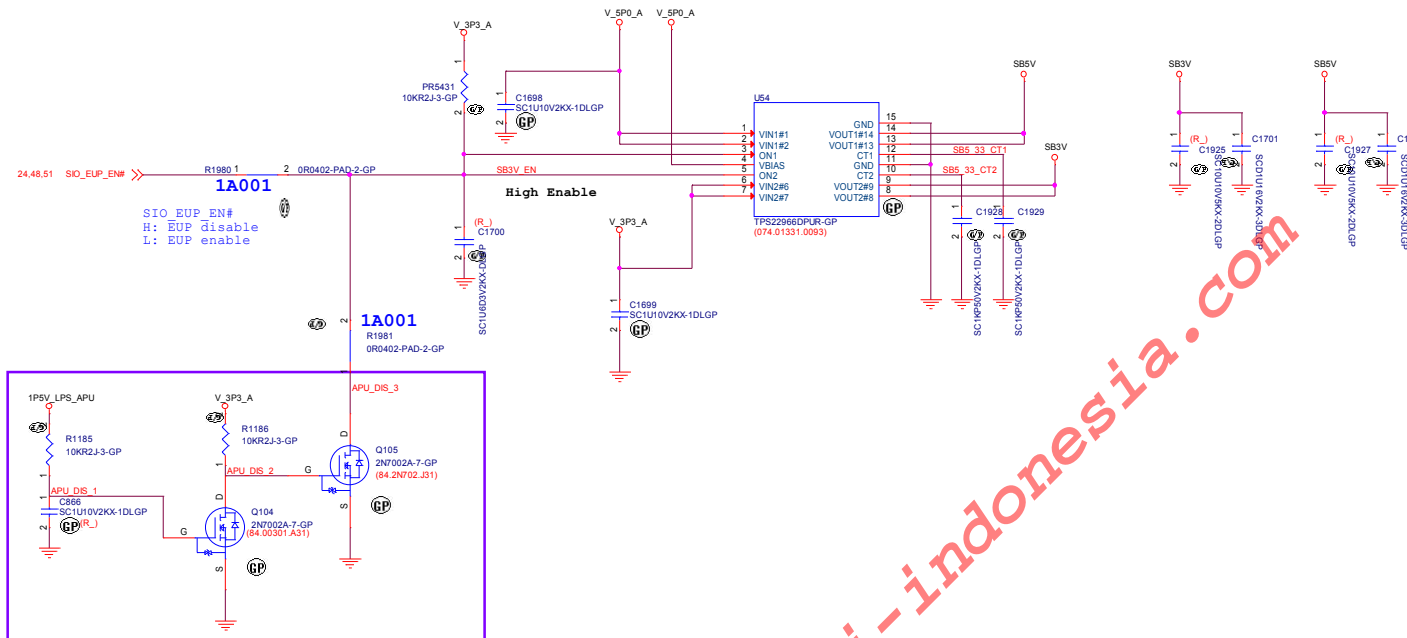
Run Power(0.95_S5->0.95_S0)



Run Power(5V_S0,3.3V_S0,1.8V_S0)



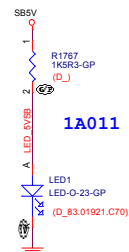
0618 Eric modfiy from Braswell EUP Power



*This circuit is used to prevent turn on system when RTC removal
,and Q104 can only use MOS to prevent RTC power exhaust*

VCC5SB LED

0811 Eric delete 5V always LED



<Variant Name>

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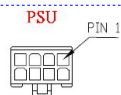
Wistron Incorporated
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Hsichih, Taipei

File 041_DSW_POWER_CTL

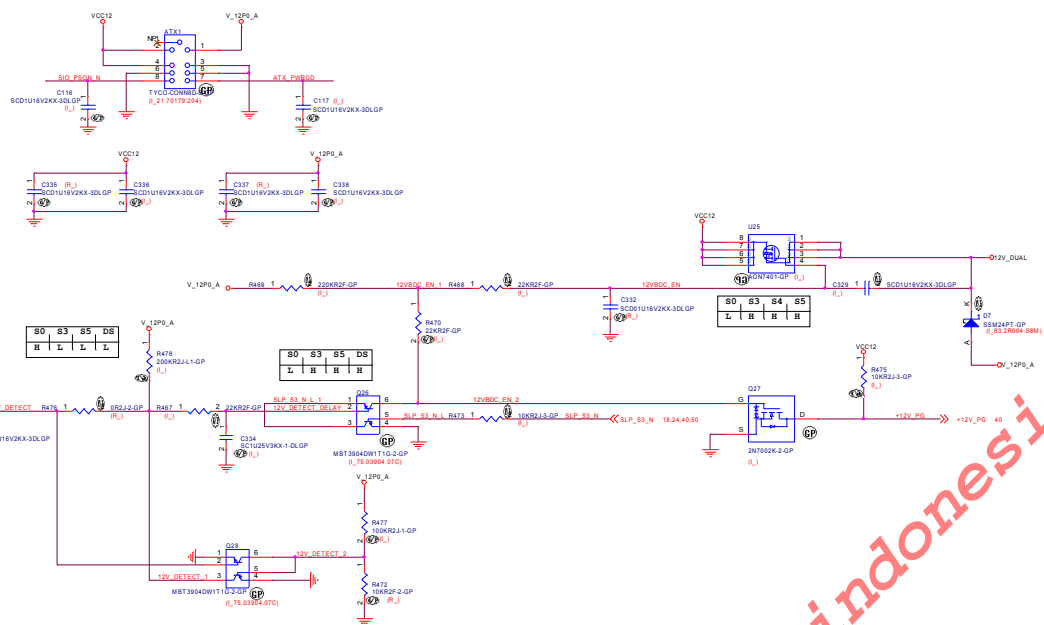
Size	Document Number	Rev
C	Rosa_Lby-MT	A00

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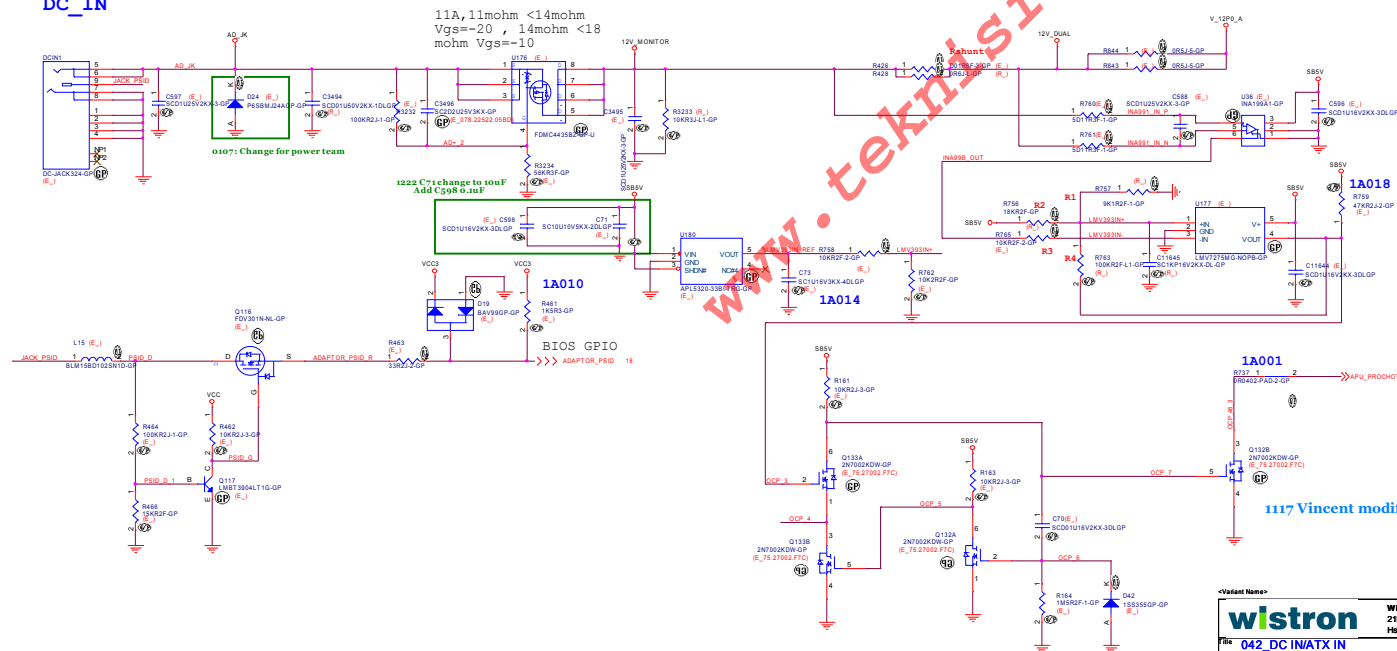
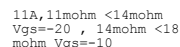
ATX CONNECTOR



1	+12VSB	5	COM
2	+12VBDC	6	COM
3	COM	7	P_OK
4	+12VBDC	8	PS_ON



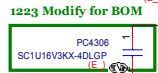
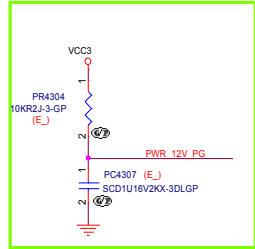
DC IN



1117 Vincent modify

VCC12

Vo=11.99V
VO=11.87V~12.11V
OVP=13.19V
OCP=5.44A
Iomax=2.5A
Fsw=300KHz



SIS420DN
84.00412.037
Vds=30V
Rds(on)=24~30 mohm@Vgs=4.5V

SIS780DN
84.00780.037
Vds=30V
Rds(on)=14.5~17.5mohm@VGS=4.5V

Vin ripple current Imax=4A

1015 Vincent Delete

1015 Vincent Modify

Iomax=2.5A
OCP>4.5A

1226: power team modify OCP

Rocset=Iocth*Rdson/Iocset
Iocp=(10uA*9.53K)/17.5mohm=5.44A

From SIO

$$V_{out} = 0.8 * (R1 + R2) / R2$$

$$= 11.99V$$

$$V_{out} = 0.792 * (R1 + R2) / R2$$

$$= 11.87V$$

$$V_{out} = 0.808 * (R1 + R2) / R2$$

$$= 12.11V$$

$$OVP = 0.88 * (R1 + R2) / R2$$

$$= 13.19V$$

<Variant Name>

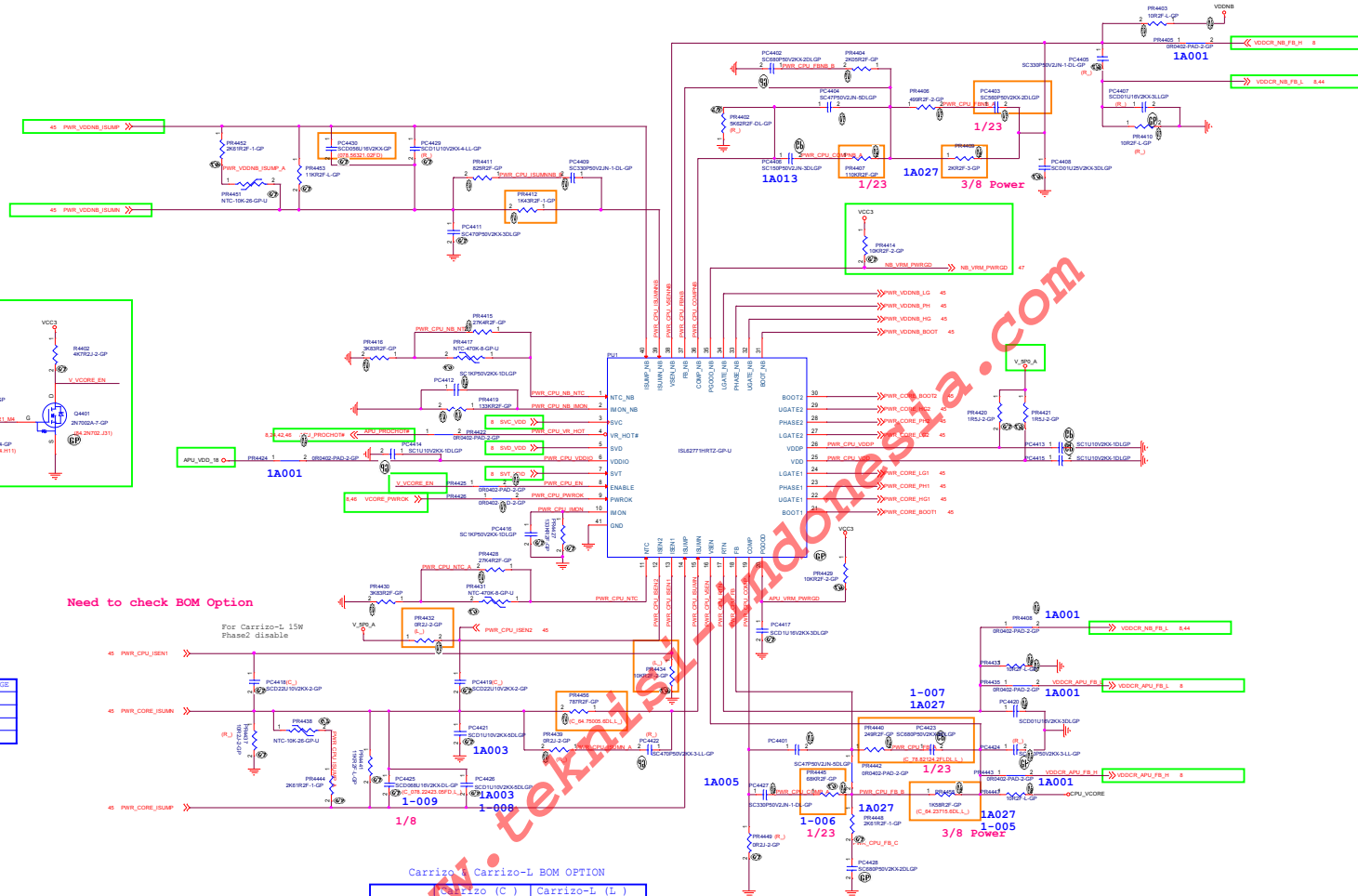
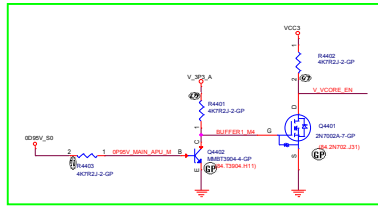
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Title 043_PWR_12V_NCP1589A

Size Custom
Document Number Rose_LJA-MT

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Need to check BOM Option

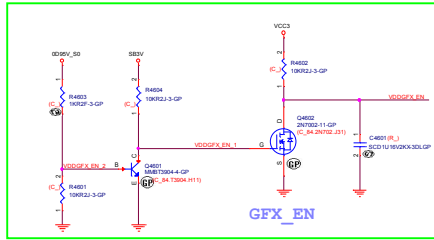
For Carrizo-L 15W Phase2 disable

SVC	SVD	BOOT VOLTAGE
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

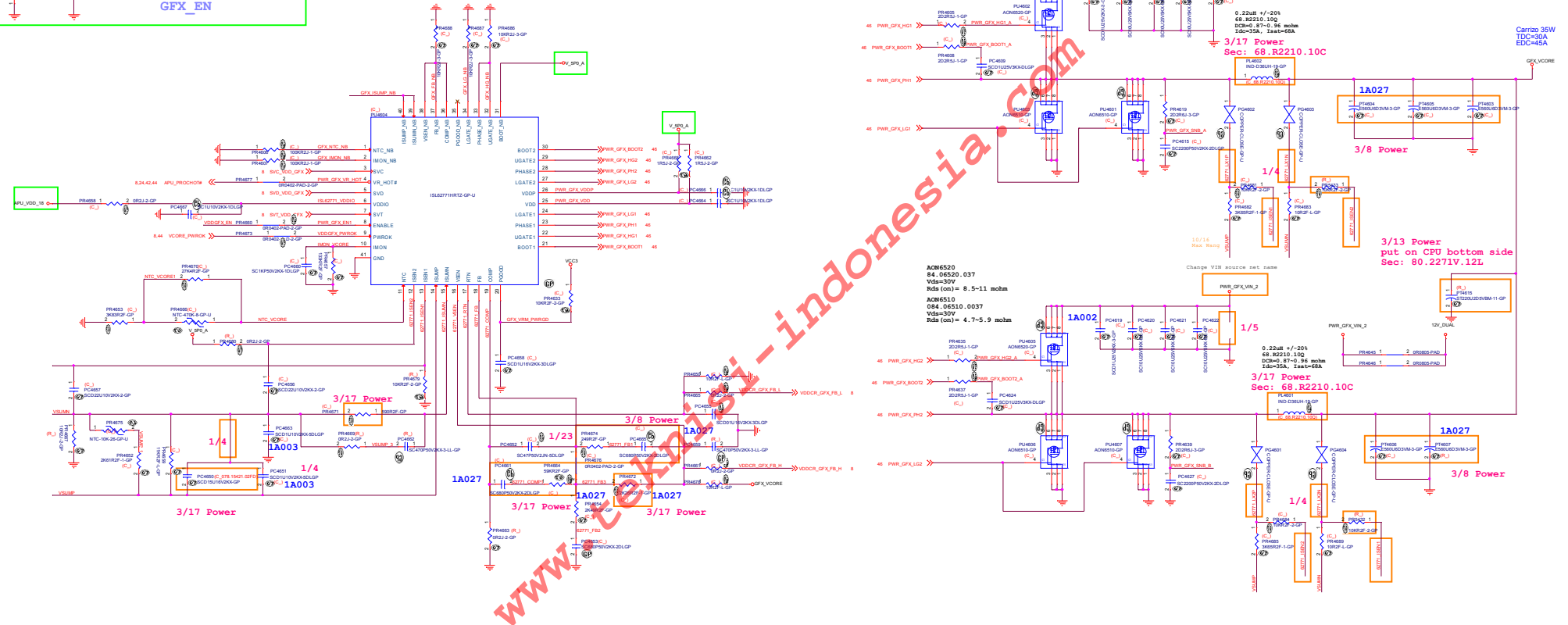
	Carrizo (C_)	Carrizo-L (L_)
PR4456	2.37K	1.58K
PR4456	750	757
PR4456	NI	PUP
PR4456	NI	PUP
PC4419	PUP	NI
PC4418	PUP	NI
PC4426	PUP	PUP



power team
EE



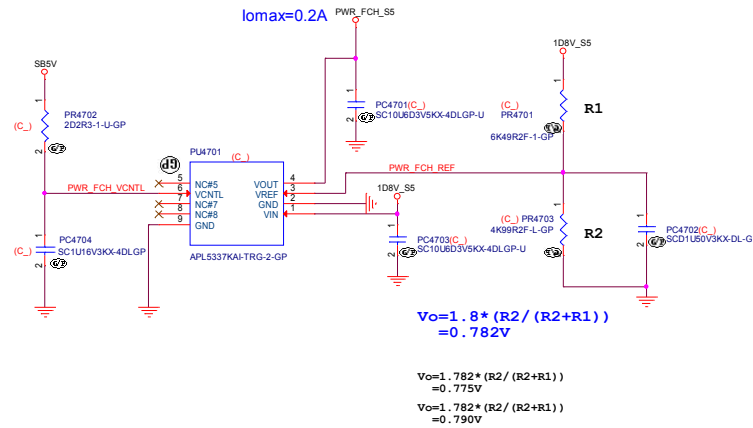
OVP=VID+300mV (min)
Carriizo 35W, OCP=68A
Carriizo 35W, TDC=30A, EDC=45A



V_1P8_S5 --> V_0P775_S5

0.775V_S5

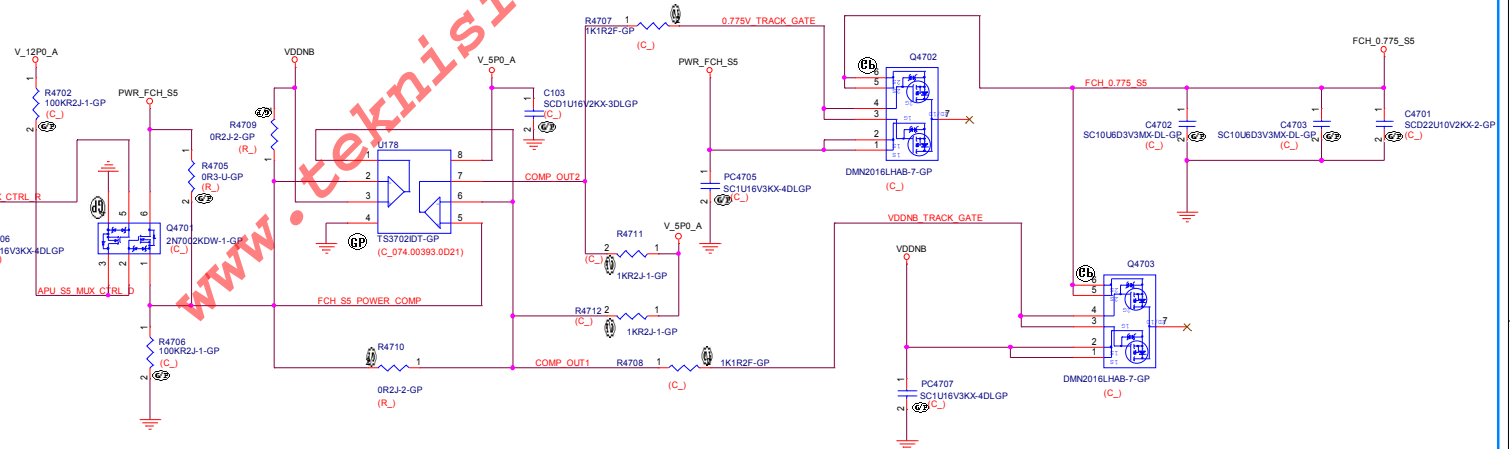
Vo=0.782V
Vo=0.775V~0.79V
OCP=3A
Iomax=0.12A



VDDCR_FCH_ALW

1016 Vincent Modify

S5 MUX APU:
High:S3 to S0 VDDCR_FCH_S5=APU_VDDNB
LOW:S0 to S3 VDDCR_FCH_S5=0D775_S5



<Variant Name>

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
File 047_VDDCR_FCH_S5			
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power team
EE

V_0P95_A

Vo=0.9557V
VO=0.951V~0.9605V
OVP=1.141V
OCP~16.275A
Iomax=9.3A
Fsw=290KHz

AON6520
84.06520.037
Vds=30V
Rds(on)= 8.5~11 mohm
AON6510
084.06510.0037
Vds=30V
Rds(on)= 4.7~5.9 mohm

Iomax=9.3A
OCP>13.95A

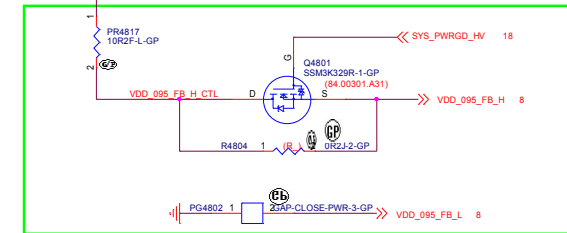
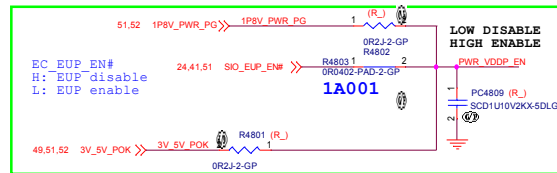
1226: power team modify

$$V_{out} = 0.704 * (1 + R1/R2) = 0.704 * (1 + 11.8/33) = 0.9557V$$

$$V_{out} = 0.7005 * (1 + R1/R2) / R2 = 0.951V$$

$$V_{out} = 0.7075 * (1 + R1/R2) / R2 = 0.9605V$$

	PR4801
Carrizo-L	11.8Kohm
Carrizo	16.2Kohm



power team
EE

V_3P3_A

Vo=3.33V
VO=3.2976~3.38V
OVP=3.56V
OCP=14.25A
Iomax=7.8A
Fsw=375KHz

V_5P0_A

Vo=5.0V
VO=4.95V~5.075V
OVP=5.346V
OCP=11.725A
Iomax=6.7A
Fsw=325KHz

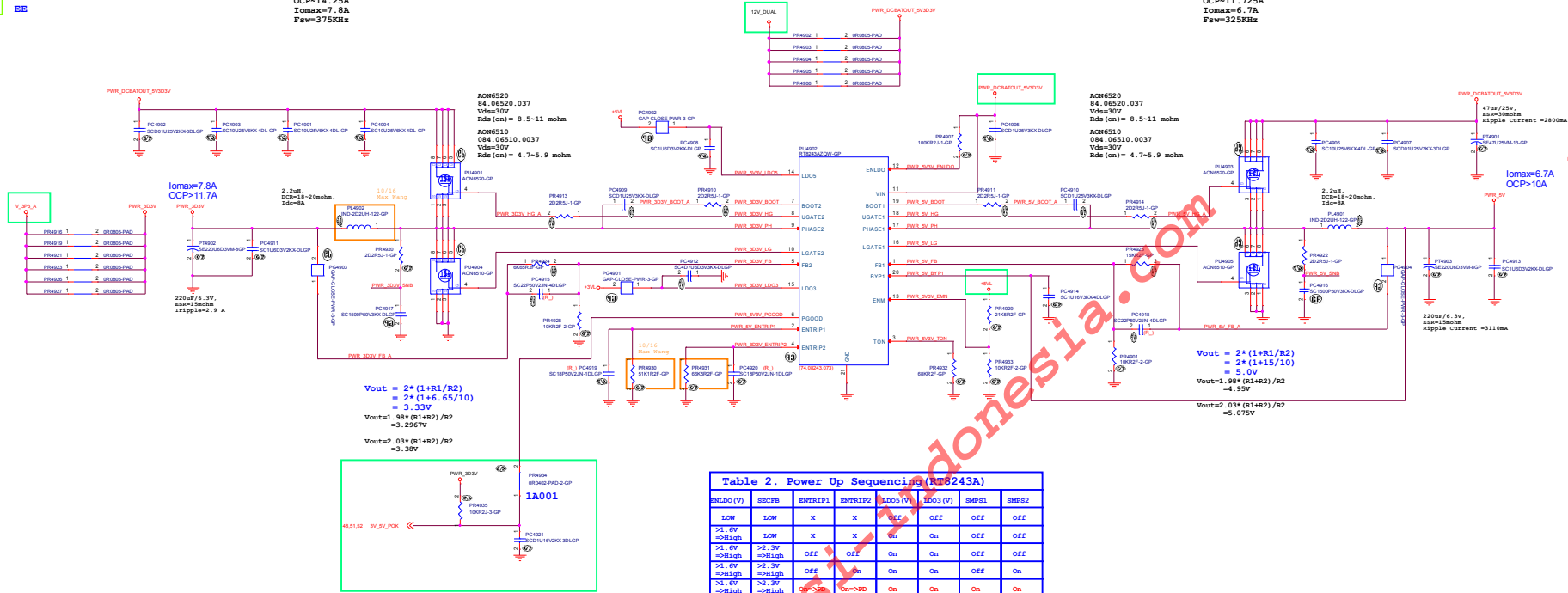


Table 2. Power Up Sequencing (RT8243A)

ENLDO (V)	SELFB	ENTRIP1	ENTRIP2	LDOS (V)	LDOS (V)	EMP81	EMP82
LOW	LOW	X	X	OFF	OFF	OFF	OFF
>1.6V >High	LOW	X	X	On	On	OFF	OFF
>1.6V >High	>2.3V >High	OFF	OFF	On	On	OFF	OFF
>1.6V >High	>2.3V >High	OFF	On	On	On	OFF	On
>1.6V >High	>2.3V >High	On	On	On	On	On	On
>1.6V >High	>2.3V >High	On	On	On	On	On	On

V_1P35_S3

Vo=1.369V
VO=1.3545V~1.3837V
OVP=1.49V
OCP~17.5A
Iomax=10A
Fsw=400KHz

power team
EE

AON6520
84.06520.037
Vds=30V
Rds(on)= 8.5~11 mohm
AON6510
084.06510.0037
Vds=30V
Rds(on)= 4.7~5.9 mohm

Iomax= 10A
OCP>15A

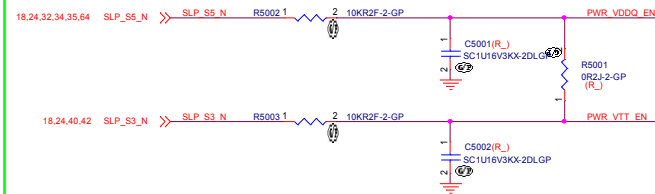
0.675V
Iomax: 1A

1226: modify for power team
 $V_{out} = 0.75 \times (1 + R1/R2)$
 $= 0.75 \times (1 + 40.2/48.7)$
 $= 1.369V$

$V_{out} = 0.742 \times (R1 + R2) / R2$
 $= 1.3545V$

$V_{out} = 0.758 \times (R1 + R2) / R2$
 $= 1.3837V$

S0	S3	S5	DS
H	H	L	L



<Variant Name>

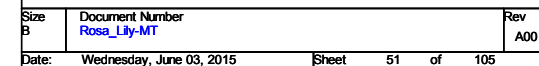
wistron

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File 050_DDR/0.675V_PWR (RT8207M)

Size C Document Number Rev A00

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V_1P8_A--> V_1P5_A

$I_{max}=0.1A$



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Title	052 1D5V S5 (APL5930)
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Size	Document Number
B	Rosa_Lily-MT

Date: Wednesday, June 03, 2015

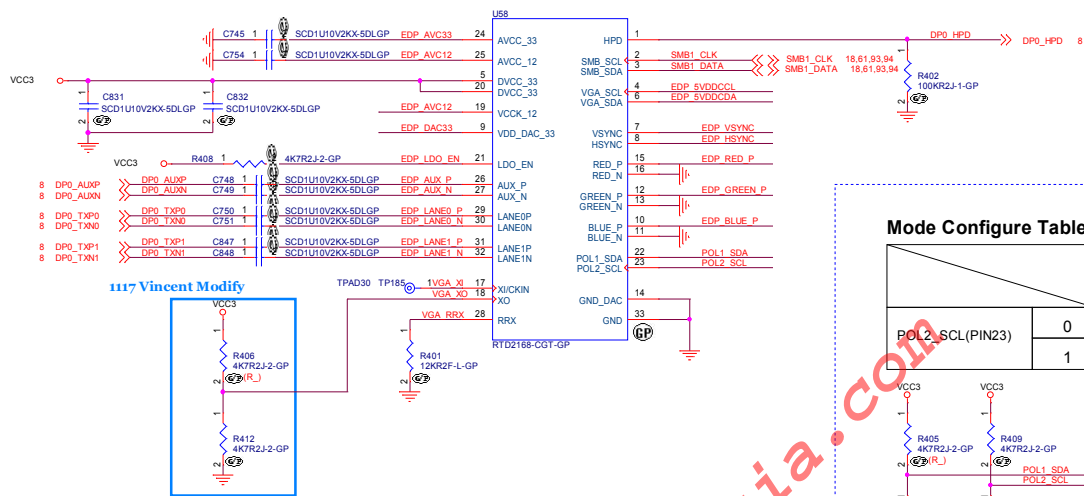
Rev	
A00	

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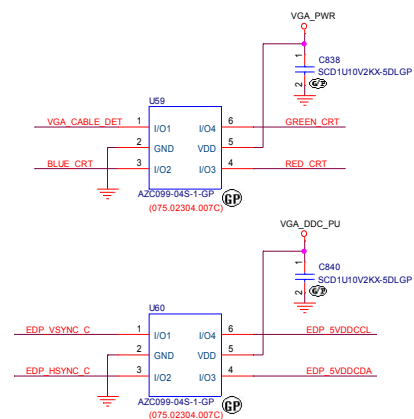
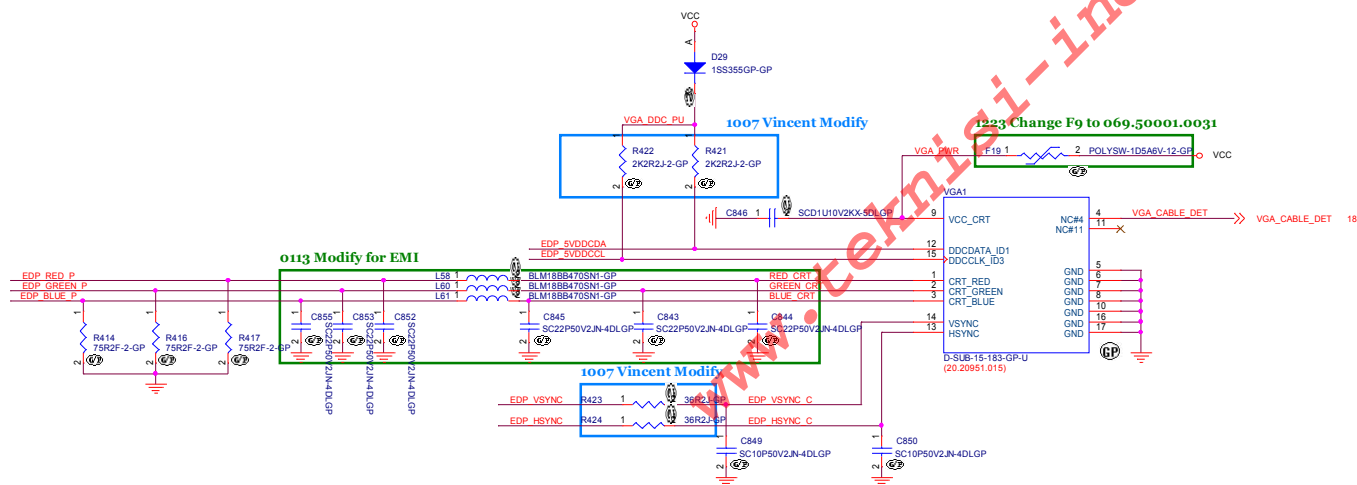
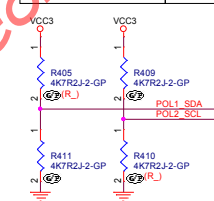
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		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

ROM ONLY Mode : PIN22 pull low, PIN23 pull high
EP Mode : PIN22 pull high, PIN23 pull low
EEPROM Mode : PIN22 pull high, PIN23 pull high

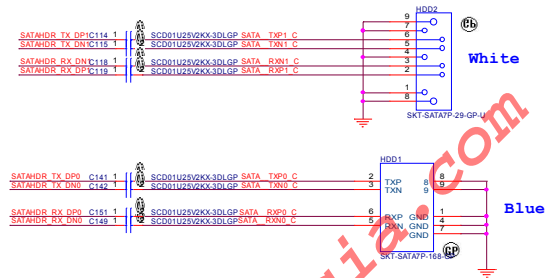


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SATA

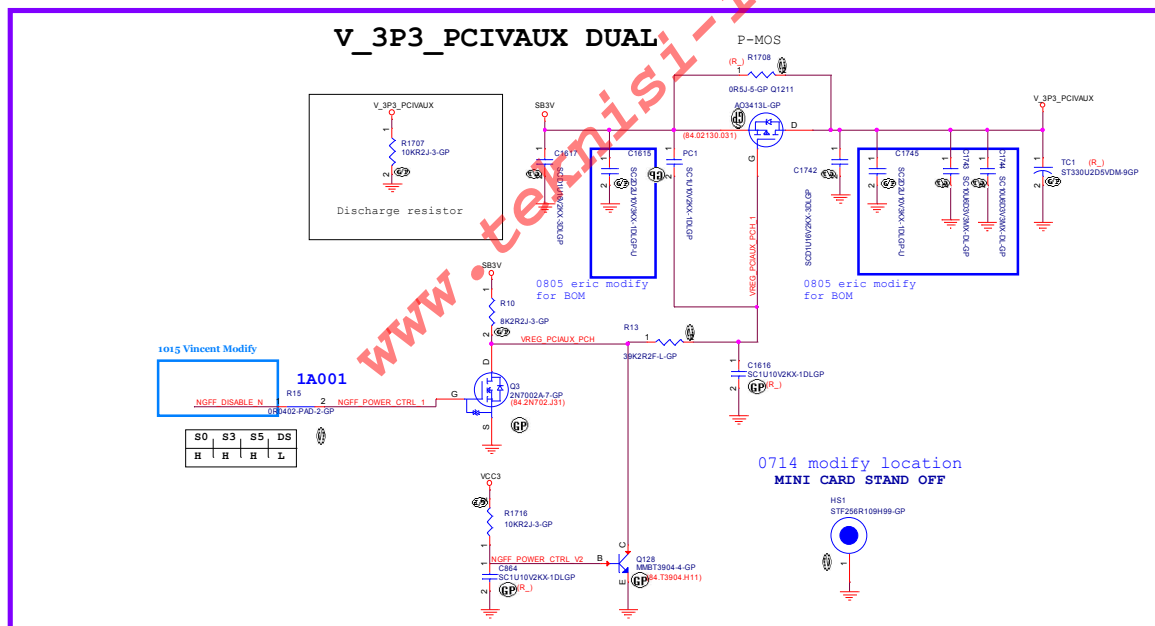
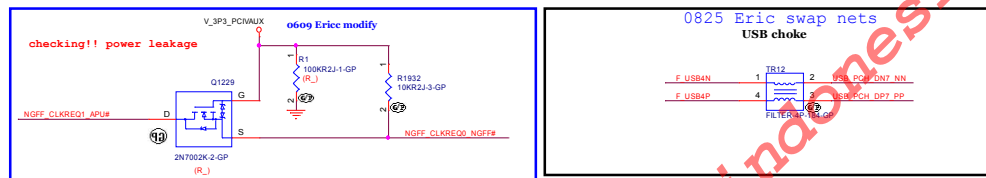
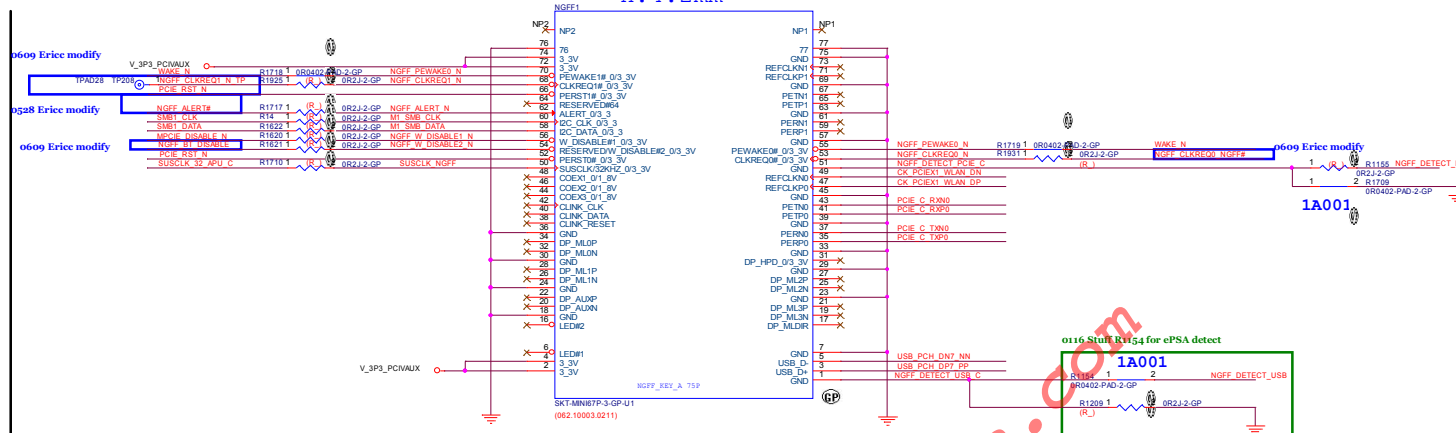
16 SATAHDR_RX_DP0
16 SATAHDR_RX_DN0
16 SATAHDR_TX_DN0
16 SATAHDR_TX_DP0
16 SATAHDR_RX_DP1
16 SATAHDR_RX_DN1
16 SATAHDR_TX_DN1
16 SATAHDR_TX_DP1




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NGFF(A Key)

H: 4.2mm




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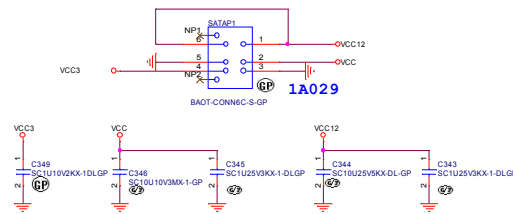


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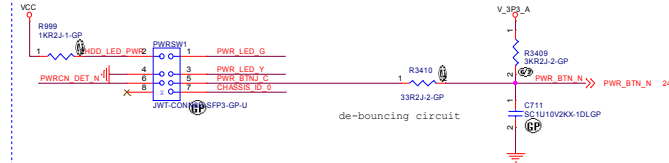
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Title Reserved			
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SATA POWER CONNECTOR



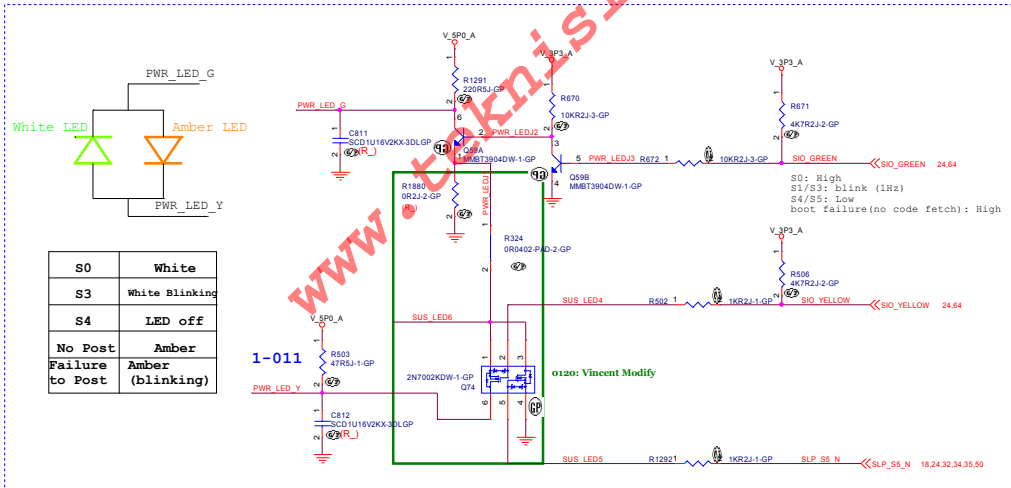
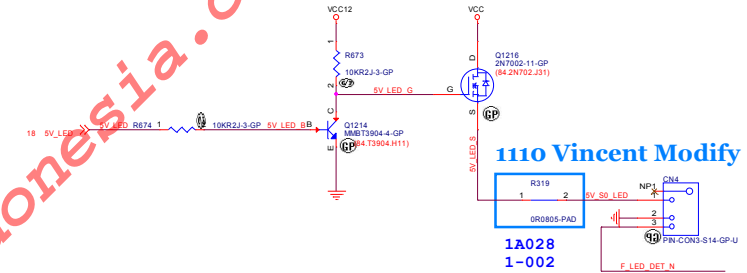
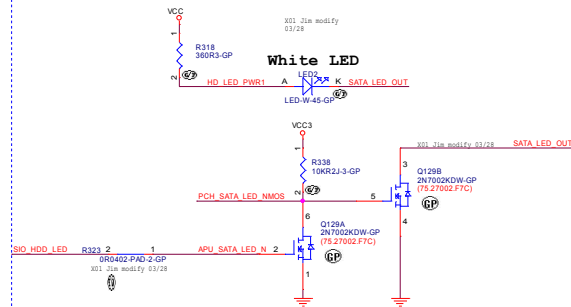
POWER BUTTON



HD_LED

16 APU_SATA_LED_N >>>
24 SIO_HDD_LED >>>
24.84 SIO_YELLOW >>>
24.84 SIO_GREEN >>>


HDD LED



S0	White
S3	White Blinking
S4	LED off
No Post	Amber
Failure to Post	Amber (blinking)

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<Variant Name>



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Title

Reserved

Size
B

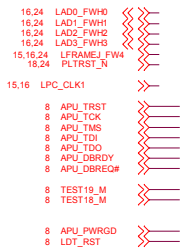
Document Number
[Rosa_Lily-MT](#)

Rev
A00

Date: Wednesday, June 03, 2015

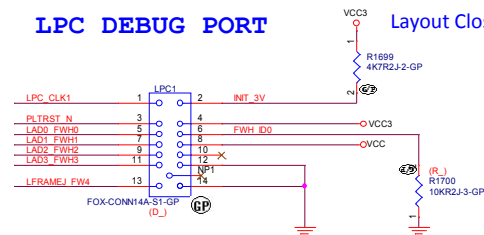
Sheet 67 of 105

LPC DEBUG PORT



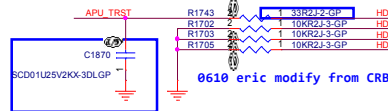
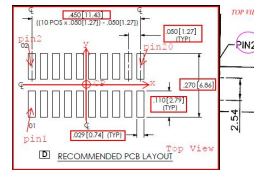
LPC DEBUG PORT

Layout Close SIO



Pin height 2.3mm

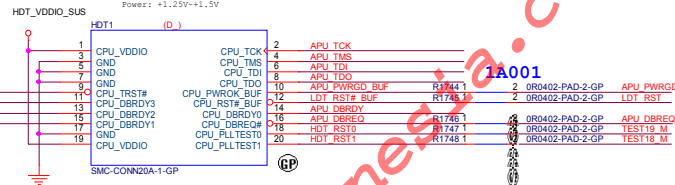
Follow Eagle



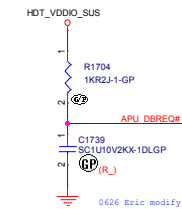
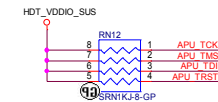
0610 eric modify from CRB

Debug Header

Power: +1.25V~+1.5V



1A001



0626 Eric modify

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Title Reserved			
Size A4	Document Number Rosa_Lily-MT		Rev A00
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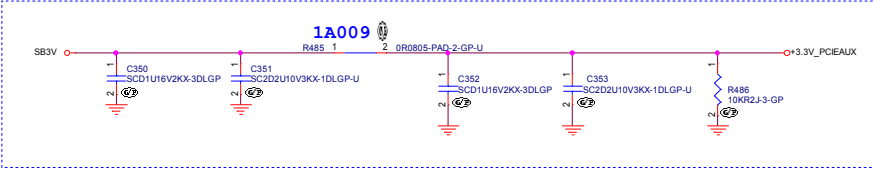
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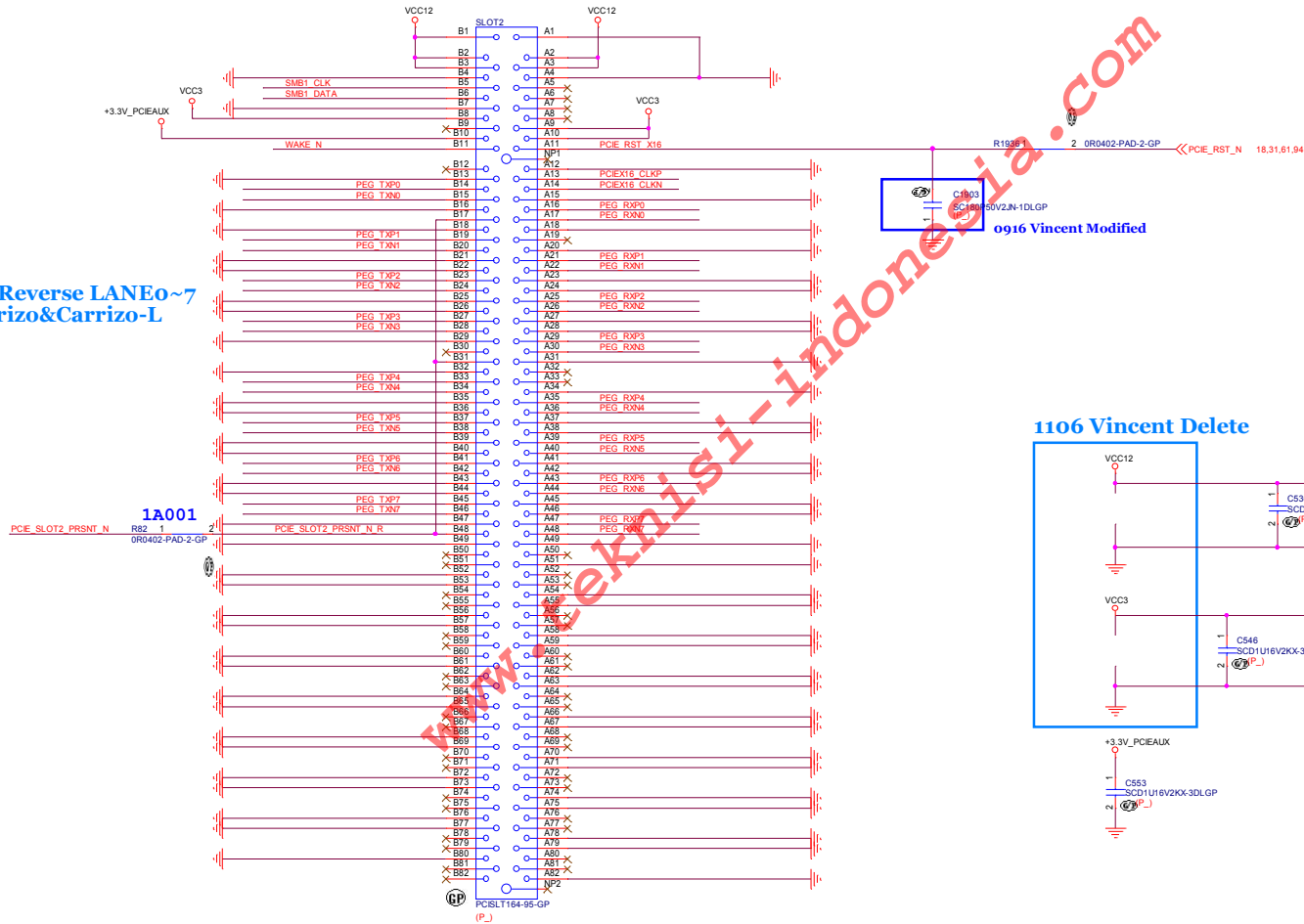
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File Reserved			
Size C	Document Number Rosa_Lby-MT		Rev A00
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Layout Colse to PCI-e
02/23



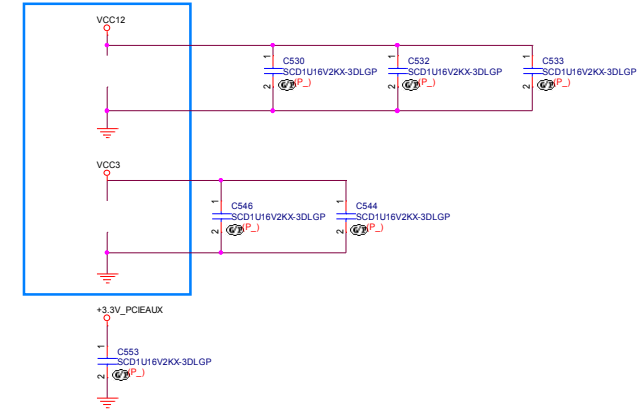
0924 Vincent Modified



1009 Vincent Reverse LANE0~7
for co-lay Carrizo&Carrizo-L

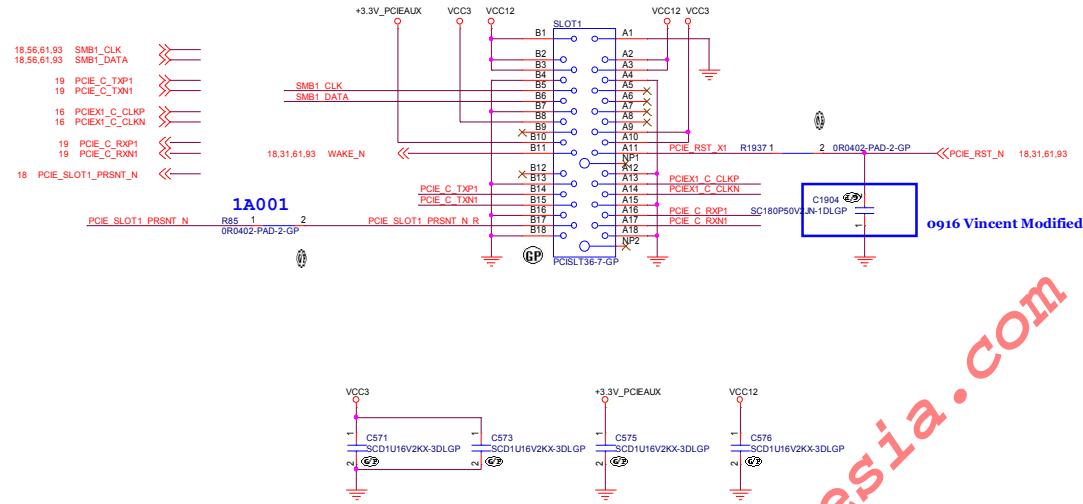
0916 Vincent Modified

1106 Vincent Delete



0924 Vincent Modified

PCIEX1 CONN




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<Variant Name>

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Size C	Document Number Rose_Lily-MT		Rev A00
Date:	Wednesday, June 03, 2015	Sheet	94 of 105

<Variant Name>

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5	4	3	2	1
D				
C				
B				
A				

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<Variant Name>			
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5	4	3	2	1
D				
C				
B				
A				

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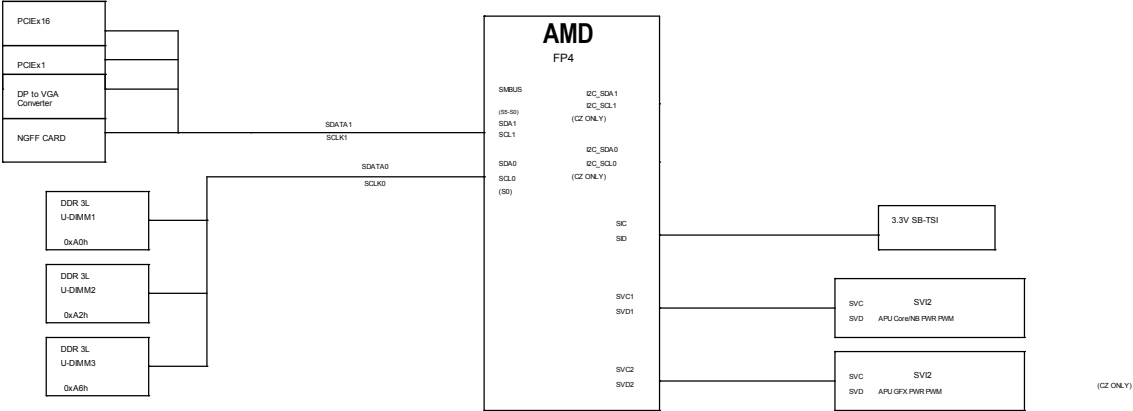
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Size A4	Document Number Rosa_Lily-MT		Rev A00
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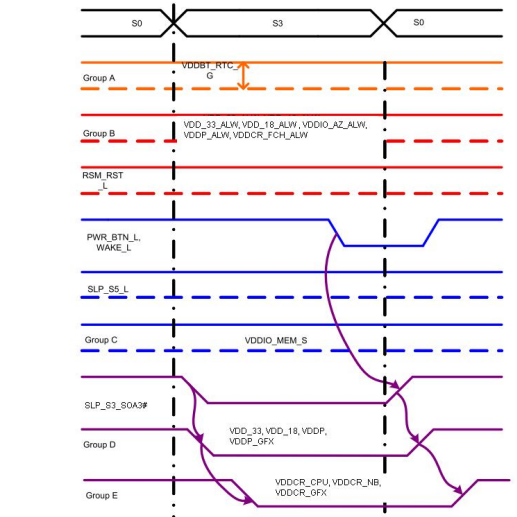
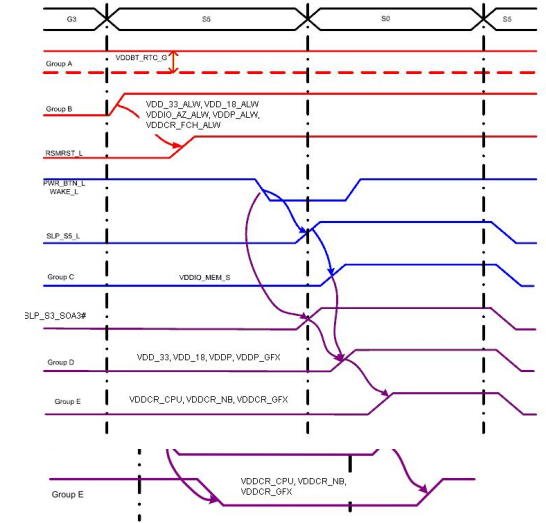
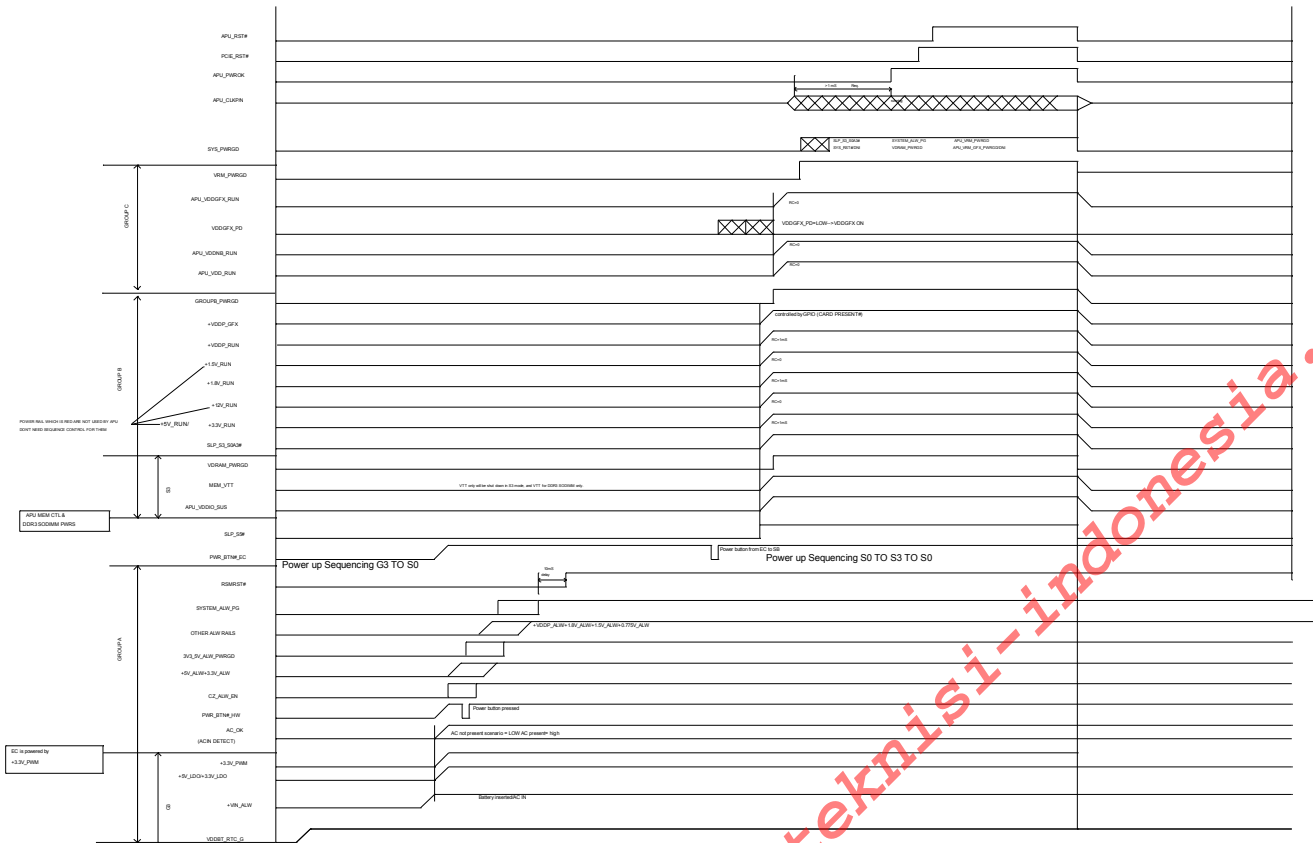
叠层编号	6-1.6-11i	注意事项	1. Impedance Control tolerance +/- 10%				
完成板厚 (mm)	1.6 ± 0.16		2. Coupon 製作方式及 Impedance report 請依照 Wistron 規範製作				
Stack up		Impedance Request List					
		Layer Spec	L1 (Ref. Plane) ※ 1	L3 (Ref. Plane)	L4 (Ref. Plane)	L6 (Ref. Plane)	
		Single Ended Type (Trace width : mil)					
L1	TOP		34Ω	9.5(L2)※ 4	11.5 (L2/L5)	11.5 (L3/L5);11.5(L2/L5)	9.5 (L5)※ 4
	PP		35Ω	9.5(L2)※ 4	11 (L2/L5)	11 (L3/L5);11 (L2/L5)	9.5 (L5)※ 4
L2	G/P ※ 3		37.5Ω	8 (L2)	9.5 (L2/L5)	9.5 (L3/L5);9.5 (L2/L5)	8 (L5)
	Core		39Ω	7.5 (L2)	9 (L2/L5)	9 (L3/L5);9 (L2/L5)	7.5 (L5)
			40Ω	7 (L2)	8 (L2/L5)	8 (L3/L5);8 (L2/L5)	7 (L5)
L3	S/G/P		42Ω	6.5 (L2)	7.5 (L2/L5)	7.5 (L3/L5);7.5 (L2/L5)	6.5 (L5)
	PP		45Ω	5.5 (L2)	6.5 (L2/L5)	6.5 (L3/L5);6.5 (L2/L5)	5.5 (L5)
L4	Signal		50Ω	4.5 (L2)	5 (L2/L5)	5 (L3/L5);5 (L2/L5)	4.5 (L5)
	Core		55Ω	3.5 (L2) ※ 2	4 (L2/L5)	4 (L3/L5);4 (L2/L5)	3.5 (L5) ※ 2
L5	G/P		60Ω	NA	NA	NA	NA
	PP						
L6	Bottom						
		Differential Type (Trace width/Space width/Trace width: mil)					
			110Ω	NA	NA	NA	NA
			100Ω	4/10/4(L2)	4/9/4(L2/L5)	4/9/4(L3/L5);4/9/4(L2/L5)	4/10/4(L5)
			95Ω	4/6.5/4(L2)	4/6.5/4(L2/L5)	4/6.5/4(L3/L5);4/6.5/4(L2/L5)	4/6.5/4(L5)
			93Ω	4/6/4(L2)	4/6/4(L2/L5)	4/6/4(L3/L5);4/6/4(L2/L5)	4/6/4(L5)
			90Ω	4/5/4(L2)	4/5/4(L2/L5);5/8/5(L2/L5)	4/5/4(L3/L5);5/8/5(L3/L5);4/5/4(L2/L5);5/8/5(L2/L5)	4/5/4(L5)
			85Ω	4/4/4(L2); 5/6/5(L2)	4/4/4(L2/L5);5/6/5(L2/L5)	4/4/4(L3/L5);5/6/5(L3/L5);4/4/4(L2/L5);5/6/5(L2/L5)	4/4/4(L5); 5/6/5(L5)
			80Ω	5.5/5/5.5(L2); 6/6/6(L2)	5/4/5(L2/L5)	5/4/5(L3/L5);5/4/5(L2/L5)	5.5/5/5.5(L5); 6/6/6(L5)
			72Ω	7/5.5/7 (L2);6/4/6(L2)	7/4.5/7(L2/L5)	7/4.5/7(L3/L5);7/4.5/7(L2/L5)	7/5.5/7 (L5);6/4/6(L5)
			70Ω	7/5/7 (L2)	7/4/7(L2/L5)	7/4/7(L3/L5);7/4/7(L2/L5)	7/5/7 (L5)
			68Ω	7/4/7 (L2)	7.5/4/7.5(L2/L5)	7.5/4/7.5(L3/L5);7.5/4/7.5(L2/L5)	7/4/7(L5)
			65Ω	8/4/8 (L2)	9/5/9(L2/L5)	9/5/9(L3/L5);9/5/9(L2/L5)	8/4/8(L5)
		Remark:					
		※ 1: "Ref. Plane" means the reference plane of the traces.					
		※ 2: Trace space should be wider than 4mil.					
		※ 3: G is GND, P is PWR					
		※ 4: Only choose one signal to control on layer L1&L6					
Total	60.2						

SMBus Block Diagram

ALL SLAVE ADDRESS IS 8-BIT INCLUDING W/R BIT
SLAVE ADDRESS FOR SLOT/HEADER PLEASE REFER TO MODULE SPEC



FROM AMD CRB BOARD



Power on Sequence required:

- There is no sequencing requirement between power supplies within the individual power groups.
- All power supplies in Group A must be stable and within specifications for 5 seconds before any power supply in Power sequencing Group B is greater than 10% of its specified minimum operating voltage.
- All power supplies in Group B must be stable and within specifications before any power supply in Power sequencing Group C is greater than 10% of its specified minimum operating voltage.
- All power supplies in Group C must be stable and within specifications before any power supply in Power sequencing Group D is greater than 10% of its specified minimum operating voltage.

